POST-Probe PCI

TECHNICAL MANUAL

by

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Introduction

About Micro2000 Inc.

Micro 2000 was formed in September 1990 to supply the PC industry with top-quality diagnostics, which were virtually non-existent at the time for that segment of the industry. Since then, the company has maintained its position of leadership through outstanding technical support and by staying consistently on the cutting edge throughout the rapid advances in PC technology that continue to occur.

Whether it is PC diagnostic software or hardware, educational materials or network administrative tools, you can trust all Micro 2000 products to be state-of-the-art and to be the highest quality products of their kind available anywhere.

About Post Probe

The Post Probe is the tool to quickly diagnose any IBM-compatible PC that will not boot up. The Post Probe is a printed circuit card that plugs into any vacant bus slot on the computer's motherboard. It can be used with the ISA bus, EISA, or the newer PCI bus. The Post Probe monitors the voltages, bus signals, and the computer's Post, or Power-On-Self-Test, and shows the results with various LED and 7-segment displays.

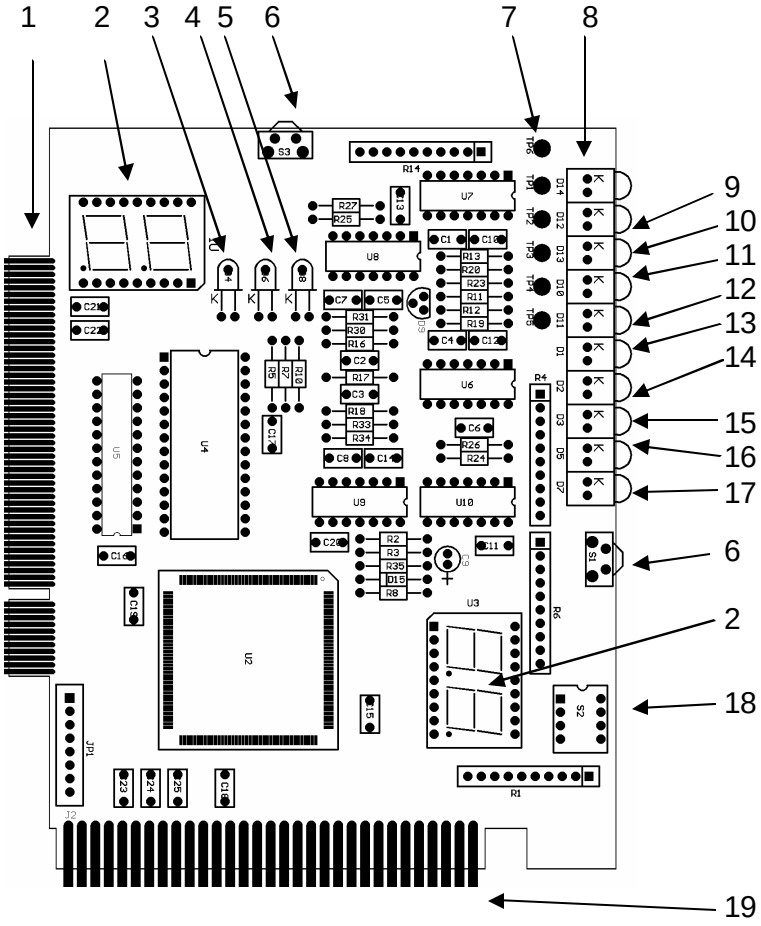
A computer when powering up will go through a series of steps in the BIOS to test the computer's subsystems. As it does each step, it generates a code for that step, called a POST code. The code varies according to the manufacturer and version of the BIOS. Post Probe reads these codes, and if the BIOS fails to get all the way through the tests, the code displayed will show where the Power-On-Self-Test halted. There is also a button that allows you to step through the codes one at a time.

The LED display, the code tables for your type of BIOS (in Chapter 3 of this manual), and the diagnostic procedures in Chapter 2 will allow you to diagnose the failure, in many cases to the exact component that

needs to be replaced. Together with Micro 2000's Micro-Scope diagnostic software, you will have the arsenal to conquer virtually any PC computer problem you may encounter.

Post Probe Features

1. PCI CONNECTOR	11. +12 VDC
2. 7-SEGMENT DISPLAY	12. –12 VDC
3. OSC. LED	13. CLK LED
4. RESET LED	14. FRAME/ SMEMR LED
5. ALE LED	15. IRDY/ SMEMW LED
6. STEPPING SWITCH	16. TRDY/ IOW LED
7. VOLTAGE TEST POINTS	17. DEVSEL/ IOR LED
8. 3.3 VDC	18. DIP SWITCH
9. +5 VDC	19. ISA CONNECTOR
10. –5 VDC	



POST-Probe Physical Layout

Notice: The Post Probe card is designed to be used for the short period of time that the computer is performing its Power-On Self Test during boot-up. Leaving the card inserted into the computer for extended periods of time may cause the card to be damaged through overheating, and will void the warranty for the Post Probe.

Chapter 1
Using The POST-Probe

Installing the Card

You will notice that the Post Probe card has two edge connectors. One of these is for the ISA or EISA type bus, and the other is for the newer PCI bus. If your motherboard has slots for both types of bus, you should use both. The POST codes will be the same, but the individual LEDs monitor different signals on each bus. If only one bus is available, it will be apparent which one to use.

If neither connector fits in the bus slot, you have encountered a third type, called the MCA bus. MCA stands for "Micro-Channel Architecture, which is a bus standard developed by IBM for their PS-1 and PS-2 systems. The Post Probe can also be used in this type of bus, by first plugging the ISA connector into an MCA adapter card, which is available from Micro 2000.

To install, turn off the computer and open the case. Although not required, it is usually a good idea to begin by removing all of the adapter cards plugged into the motherboard's bus slots in order to narrow down the source of trouble, because one of these cards could be shorting out the bus.

Now, orient the Post Probe card so that the row of LEDs are facing up (for PCI) or toward the front of the computer (for ISA). If there is any doubt about the orientation of the card, there are arrows adjacent to each of the connectors. The arrow for the connector in use should be pointing toward the nearest edge of the motherboard.

Push the Post Probe gently and evenly into a vacant bus slot. When the card bottoms out in the slot, check along the top edge of the slot to ensure that the card is straight and even. You may need to remove a plate or bracket covering the opening at the back of the computer, by taking out the screw at the top of the bracket. Once the card is installed, remove your hands and any tools from the computer case,

and turn on the power. The computer will begin its Power-On-Self-Test.

What do all those lights mean?

The Post Probe has two types of displays to tell you what is happening with signals on the bus. One is the 2-digit HEX display, which we will cover in a later section. The other is a set of red, green and yellow LEDs. The green LEDs check the voltages and the red LED monitors the Reset line. The yellow LEDs each show the status of a different bus signal.

Voltages

The five green LEDs monitor the DC voltages from the power supply. Starting from the corner of the card, the voltages are +3.3 VDC, +5 VDC, -5 VDC, +12 VDC and -12 VDC. If a voltage is within a tolerance of +10% to –5%, the corresponding LED will be lit.

There are also six test points, one for ground and one for each voltage that allow easy confirmation with a voltmeter.

***Note**: There is no +3.3 VDC on the ISA bus. The PCI bus does not have –5 VDC, and some PCI models also are missing the +3.3 VDC.*

If an LED should be lit and is not, the problem could be the power supply, the cabling from the power supply, or that the voltage line on the bus is being shorted out. If none of the LEDs light up, check the power supply, the main fuse, and the AC into the system.

Reset Line

There is one red LED on the board, located between two yellow LEDs, about 1½ inches from the edge opposite the ISA connector. This LED will light anytime the system's Reset line is activated. This normally happens only once during boot-up, but you will sometimes see the Post procedure get to a certain point and then reset, over and over. This usually means a shorted signal on the motherboard.

ISA Signals

There are seven yellow LEDs that monitor various signals on the bus. With one exception, they will monitor one function on the ISA bus and a different function on the PCI bus. The ISA functions are listed here first.

ALE (Address Latch Enable): This yellow LED (next to the Reset LED) indicates a signal from the CPU that allows the BIOS to latch addresses, such as memory addresses. This LED should blink periodically during the Post. If it does not, the main suspects are the CPU, the DMA circuit, Bus Controller or the Clock Generator. This LED has no function on the PCI bus.

I/O READ: This LED will be lit anytime the BIOS tries to read from an I/O device such as the hard drive, floppy, keyboard etc. If an I/O device is failing, this will give you a clue whether the fault is with the device or its controller (light blinks on) or something on the motherboard such as the BIOS or the DMA chip (light doesn't go on). On the backside of the board, this LED is labeled DEVS / IOR.

I/O WRITE: Lights when the BIOS writes to a device, and provides the same troubleshooting clues as the I/O READ. Labeled TRDY / IOW.

MEMORY WRITE: BIOS checks RAM by writing to memory and then reading what was written. This LED blinks during the write. If it doesn't, suspect the BIOS or the DMA chip. Label is IRDY / SMEMW.

MEMORY READ: If MEMORY WRITE blinks but this one doesn't, try replacing the RAM. Labeled FRAME / SMEMR.

CLOCK (CLK): This monitors the main system timing signal. It should blink rapidly and continuously, and may appear to be steady on. If not lit, check the crystal or the clock generator chip. This signal is used on both the ISA and PCI, but is not present on the MCA bus in Micro-channel systems.

OSCILLATOR (OSC): This crystal was the main system timing in XT machines, but now is just used by the video controller for color frequency. The signal is not present on the PCI bus. On an ISA bus, the LED will blink rapidly, and may appear steady on. If not, replace the 14.138 Mhz crystal. This LED is located next to the Reset LED.

PCI Signals

CLOCK: This is the only signal, other than voltages, monitored in common with the PCI bus. It should blink rapidly or appear steadily on.

FRAME: This signal defines the timing window for data transfer on the bus. The LED should blink repeatedly during Post. If not, the problem is most likely with the PCI chipset, particularly the bus controller.

IRDY (Initiator Ready): This LED blinks when the bus recognizes a device is ready to transfer data. If this function is not working, problems will be with the PCI chipset.

TRDY (Target Ready): Blinks when the bus recognizes a device is ready to receive data. Problems could be with the PCI chipset or with an I/O device.

DEVS (Device Select): This signal shows that a device has been selected for data transfer. If no blinks, suspect the bus controller.

Switches

Stepping Switch

There are two push-button switches, located at the edges of the card opposite the connectors. Either of these allow you to step through and view the POST codes one at a time, in reverse of the sequence in which they were issued. Just push one of the buttons to progress to the previous code. There are two buttons so that one of them should be easily accessible no matter how the Post Probe card is oriented in the machine.

Please note that the button does not actually cause the Post routines to execute; rather it shows you the sequence that has already been executed. This information is valuable because the Post will not always stop on the section where the error occurred. Sometimes it goes to the next step before locking up. In other cases, the Post issues its code only after successful completion of a particular routine. If it doesn't complete, the Post will still be showing the code of the previous routine. If the BIOS has been corrupted, you may even find the Post executing steps out of sequence, and the stepper switch is the only way to easily determine exactly what is happening.

DIP Switch

The four-position dual inline pin (DIP) switch on the Post Probe card sets the I/O port that the card reads to get its Post codes. Most systems output their codes to I/O Port 80, but there are exceptions, as noted in the table.

Switch #	1234	
Port 80	1111	Most ISA, EISA & PCI systems (default)
Port 84	0111	Compaq systems
Port 90	1101	PS2 models 25 and 30
Port 190	1100	Any BIOS using Port 190
Port 300	1011	Award systems with EISA bus
Port 380	1010	Compaq systems
Port 680	1001	MCA systems
All Above	1000	When in doubt, try this.
Test	0000	Self-diagnostic mode

The settings above represent 0=OFF and 1=ON. This chart is also silk-screened onto the back of the Post Probe. Be aware there are some early versions of the card that show 0=ON and 1=OFF.

The self-diagnostic mode will put the display into a continuous loop, which won't stop unless it encounters a card malfunction. If this occurs, contact technical support.

The Hex Display

Each brand and version of BIOS has its own Post routine that it goes through on boot-up, and each has its own set of codes that it puts out for the various parts of the Post. Even though all computers are prone to the same types of problems, the codes will vary and need to be interpreted. Fortunately however, all BIOS' put out the codes in hexadecimal format.

These hexadecimal codes are displayed by the 7-segment Hex display. There are two digits in the display, because most BIOS versions use a 2-digit code. There are certain BIOS' such as the HP Vectra ES, RS and QS that use a 4-digit code, so the first two digits are displayed momentarily first, followed by the last two digits of the code.

There is a second hex display on the backside of the Post Probe card. It displays the same code, but makes it easy to read the codes no matter which way the card is oriented in the computer.

To find out what a code means, you must locate the table for your particular BIOS in Chapter 3 of this volume. The tables are in alphabetical order, by manufacturer. Each table lists the codes for those BIOS, in numerical order. Once you have found the correct table, go to the displayed code within that table.

Next to each Post Code number, you will find the manufacturer's description of the test, as well as a reference number to a particular section of the Diagnostic Procedures in Chapter 2. If you then go to that section of Chapter 2, you will see a detailed analysis of the hardware being tested in that portion of the Post procedures, and suggestions to help you isolate and fix the problem.

The tables are extensive, listing over 65 different BIOS versions from 22 manufacturers. However, new BIOS versions are being released all the time, and several BIOS manufacturers will customize the BIOS for their customers. For this reason, it is quite possible to encounter a POST code that is not included in the tables. On the other hand, a corrupted BIOS can also cause illegitimate Post Codes that are not in the table.

If the computer is damaged to the extent that Post cannot begin, the card will display a code of **AA**. This will usually require replacement of the BIOS, the CPU or the entire motherboard. The condition can also occur if an adapter card is shorting out one or more bus signals.

Certain BIOS codes are marked **Reserved** or **OEM-specific**. The BIOS manufacturer will assign these as requested by their customers, and you will need to contact your system vendor or motherboard manufacturer to find out what function has been assigned to a particular reserved code. Codes marked **Debug** are used by the manufacturer to test the chips, but are not used during normal POST.

More Post Code Resources

If you come across a code that is not in the table, or a BIOS whose table is not included in Chapter 3, please check the following websites:

http://bioscentral.com/
http://www.shopctc.com/BiosHelp/Biospostcodes/AMI.htm
http://pchell.com/hardware/beepcodes.shtml
http://computerhope.com/beep.htm
http://uktsupport.co.uk/reference/biosb.htm

If you are still unable to find the code, please contact the Micro2000 Technical Support department. We can help you determine the cause of the missing code, and you can help us keep our BIOS listing up to date.

Chapter 2
Diagnostic Procedures

Using The Codes

Next to each of the POST Codes in Chapter 3 is a Diagnostic Code, which refers to one of the sections of this chapter. Here you will find a description of the part of the system that was being tested by that portion of the POST. Where applicable, there are also suggestions for further isolating the problem. Appendix A has part numbers of some of the common motherboard chips for various functions, to help you locate the specific component.

It does not always mean you should replace that particular component. Most operations in the system require interaction from several components, and each can appear to fail if not given correct data or signals from another part. Also, the POST may not halt on the section with the defect but on the one immediately before or after. That is why we've included a button to allow you to step through the POST (see Stepper Switch in Chapter 1). However, using the POST code description, Appendix A and the information in this chapter (and sometimes a little trial and error) will nearly always allow you to determine the source of the problem.

1.0 Power Supply

Power supply voltages are monitored on the system BUS by the POST-Probe. The voltages supplied are +5V, +12V, -5V, and -12V. On machines with a PCI BUS, +3.3V is also provided on that BUS. The LEDs on the POST-Probe corresponding to each voltage will light if that voltage is within 10% of its proper value. The voltages can also be tested with a voltmeter on the POST-Probe, measuring between the test point for the voltage you wish to check and the one marked ground.

If all of the voltages are 0, the problem is the power supply, the main fuse, or the supply of 110VAC to the computer (check the cord to make sure it's plugged in).

If one or two of the voltages are bad, the cause could be a faulty supply, or the voltage line on the bus is either open or shorted. Power off, and unplug all the adapter cards and I/O devices from the motherboard. Power up and retest the voltage. If it's OK, plug things back in one at a time (power off when plugging or unplugging, of course) until the voltage fails. That's your culprit.
If the voltage is still bad with everything unplugged, disconnect the power supply from the motherboard, and check the voltages on the power supply connector. If everything checks OK, the problem is on the motherboard. If not, it's the power supply.

2.0 Motherboard

The motherboard holds the central processing unit (CPU) with its associated timing and control circuitry, and the system BUS. Also found here are the jumpers that set the system speed and sometimes other variables. On the most basic motherboard, everything else connects to the motherboard either through adapter cards, which plug into the BUS, or into a special connector on the motherboard.
Check the jumpers to make sure they are seated properly and the settings are correct. The board itself is seldom a source of failure, which usually occurs in the on-board circuitry or in one of the devices attached to the motherboard. If the problem can be isolated to a particular component, it may be possible to replace that component. However, on modern motherboards, the trend has been to combine more and more functions into large-scale integrated chips. For instance, one 82206 chip now combines the two DMA controllers, the PITs, the PICs and the RTC, whereas in older systems these were all separate chips. Many of these large-scale chips are surface-mounted with special (and expensive) equipment, and the only practical option is sometimes to replace the entire board.

2.1 System BUS

The bus is the pathway on the motherboard over which information travels between the CPU, memory, I/O devices, etc. The bus includes data lines, address lines, voltages and various other signal lines. Those

signal lines, which are monitored directly by the POST-Probe are described in the Troubleshooting section of Chapter 1. The bus could also be said to include the bus controller chip and the connectors into which the various adapter cards are plugged.

The most common bus for most of the PC's history has been the ISA (for Industry Standard Architecture) and its close cousins the EISA and VESA. New systems being sold today nearly always include the faster PCI bus, which may be used by itself or in combination with an ISA bus. The signal layouts for these various types of buses are shown in Appendix B. The USB (Universal Serial Bus) is external to the motherboard, and is not tested during the Post procedure.

The bus controller chip determines the timing of data transfers, controls whether it involves memory or I/O, and which way the transfer is going. A failure of the chip can affect any of these factors. The PCI and ISA bus will each have its own controller.

About the only other problem that occurs with the bus itself is a shorted or open signal line, which can cause any number of symptoms depending on which signal is affected. When bus defects show up in a system that was previously working, the source will most often be found in the edge connectors. Remove the adapter cards and inspect the connectors closely for bent pins or minute metal filings. Keep in mind that the problem may also be in the bus controller or other chips connected directly to the bus, or on one of the adapter cards.

2.2 CPU (Central Processing Unit)

The BIOS will try to identify the CPU and will put that ID into the CMOS. It will then have the CPU execute a series of instructions to test its functions. If you have just installed a new CPU and retained an obsolete BIOS, that could be a cause for failure. Otherwise, the problem is the CPU chip itself, which will have to be replaced. Fortunately, this chip is usually mounted in a socket or a removable housing.

2.3 NPU (Numerical Processing Unit)

Also commonly called the Math Coprocessor, this chip handles the more complicated mathematical functions, which takes some of the

load from the CPU. Since the 486, the NPU is incorporated into the CPU. In older systems, the NPU is a separate chip, which is often impossible to remove and replace without special equipment. On these systems, replacement of the entire motherboard is the most realistic option.

2.4 Chipset

This diagnostic code refers to the chip or chips on the motherboard associated with the BIOS (rather than the video chipset, covered under code 7.0). Each BIOS version is designed to work best with a particular chip set. The set would include the PIC, PIT, DMA controllers, BIOS ROM, CMOS and RTC. These are covered separately, but if the problem can't be isolated to a particular function, you will be referred to this code.

If the Chipset Initialization Test fails, you will need the specific documentation from the motherboard or BIOS manufacturer to isolate the problem, or else just replace the motherboard.
If the failure is the Chipset Wait State, you can usually cure it by changing the CMOS wait-state values for the Read, Write, Cache Read, Cache Write etc. Refer to the BIOS documentation.

2.5 System Clock

There are two aspects of the clock that are tested during the POST. First are the crystal oscillators. The main crystal generates the timing frequency for the CPU and Bus. This signal is also indicated by the CLOCK LED on the POST-Probe card. There is a second 14.318 crystal, which was the original system clock but is now just used by the PIT and video circuits. The other part is the RTC (Real Time Clock) chip, which generates the date and time information (this chip also usually contains the CMOS memory cells: see next section). You should be able to tell from the POST code description, which is being tested. Do not confuse any of these with the operating system clock. DOS and Windows both keep track of the date and time, but not until the system has successfully booted up.

2.6 CMOS

This is a section of non-volatile memory, meaning it holds its contents even when the computer is turned off, because of a long-life CMOS

battery that provides it power. Among other things, this memory holds the date and time, RAM configuration, information about the peripheral devices such as their IRQ and DMA assignments, disk drive parameters, whether the computer will start up in Real or Protected Mode, etc.

The CMOS is usually contained in the RTC chip. Any number of hardware or software glitches can corrupt the values stored in CMOS in ways that can prevent boot-up. The POST will check values stored in CMOS against data it receives from other system components, and any mismatch can cause the POST to lock up. If you can determine the incorrect value, try changing it manually through CMOS Setup and restart the computer, before replacing any hardware. If the POST continues to fail or CMOS cannot maintain its contents, the problem may be the chip but more likely will be the CMOS battery or its connections.

The battery may be inside the RTC chip or an external lithium battery. Some HP systems power the CMOS with a capacitor rather than a battery.

2.7 Extended CMOS

Newer (and more complex) systems have more variables (such as PnP) than can be stored in the normal RTC chip, and use a chip, which has an additional 2K of CMOS memory. This is labeled XCMOS.

3.0 Interrupts

The most common problem with interrupts during the POST is that two I/O devices are set to the same IRQ, or interrupt request level. Remove the most recently installed adapter card. The system will probably boot up and you can then use the Micro-Scope Diagnostic software to find out which IRQs are already in use. Jumpers on the card will allow you to change to a vacant IRQ, and you can then re-install the device. The table in Appendix A shows the allocated and available IRQs.

3.1 Programmable Interrupt Controller (PIC)

The chips that control the interrupt traffic between the CPU and various hardware devices are called Programmable Interrupt Controllers, or PICs. Each PIC can control eight interrupt lines,

designated IRQ 0 through IRQ 7. To achieve the 16 interrupt levels required by all PCs since the 286, the chips are cascaded by connecting the output of a second chip to the IRQ 2 input of the first chip. The original IRQ 2 is routed to IRQ 9 on the second chip. Any adapter card that is set to IRQ 2 is actually using IRQ 9. Some POST routines will tell you which of the two PIC chips or even which IRQ line is failing, but others just indicate a PIC failure.

3.2 PIT (Programmable Interval Timer)

This chip controls the timing of CPU interrupt sequences, and failure can show up in several places in any POST version. On older systems (286) it was also involved in the basic system timing, and could be a suspect in benchmarking errors.

4.0 BIOS

(Basic Input-Output System) These are the hard-coded instructions, contained in ROM on the motherboard, that the computer uses to get started. The BIOS executes the POST routine that tests various components and parameters of the system (and generates the POST codes). The BIOS also includes the boot loader (see 4.2).

4.1 Boot Load

As its last step, the BIOS will look for a bootable operating system and turn control of the CPU over to it. Most commonly, it will look first to the floppy drive and then to the hard drive. If a boot load error occurs, the BIOS has been unable to complete this function. The most likely causes are hardware failure of the drive or a missing boot routine. Before making any drastic repairs, first remove any floppy diskettes and see if the system boots to the hard drive. Then, insert a floppy known to contain a boot loader, and try booting again. If neither works, you might suspect a corrupt BIOS.

4.2 BIOS CHECKSUM

When all of the data in the BIOS ROM is added up, another figure is created called a checksum, which will cause the total to roll over to all zeroes. The POST does this addition all over again, and a quantity other than zero indicates that one or more bits of the ROM code have

changed, and therefore the BIOS is corrupted. Often, a corrupted BIOS will not get far enough into the POST to give this indication.

4.3 Password

A few BIOS versions will check to see if a password is stored in CMOS. This is not necessarily a problem, because the motherboard will usually have a switch or jumper that allows you to disable the password, which you can re-enter once the system has booted up.

5.0 Memory

Memory refers to storage of information in a way that is readily accessible to other parts of the system. This distinguishes it from disk drives, CDROM, etc. These devices also store information, but it must be loaded into system memory before it can be used.

The first megabyte of memory is called conventional memory, and was the maximum memory size of the first PCs. It is divided into base memory (the first 640 kilobytes) and the upper memory area (between 640k and 1 megabyte, abbreviated as UMA). Everything above 1 megabyte is called extended memory. In some older systems, there may be a section of UMA referred to as EMS, for Expanded Memory Specification.

5.1 RAM

Random Access Memory is found on narrow cards (modules) plugged into the motherboard. The chips on theses modules are Dynamic RAM or DRAM chips, meaning they must be periodically supplied power on a Refresh line in order to retain their data. RAM contents are lost whenever the system power is turned off.

Each individual chip can store from 64K to 256M bits of data. In one common configuration, each chip will provide 1 bit of data at a time to the system, and 8 chips on the module make up a byte. If there is a 9th chip, it provides the parity bit. Some DRAM chips output 4 or 8 bits at a time and will therefore have only 1 or 2 chips per module (plus parity). In all cases, the quantity and capacity of the chips used determines how many megabytes of memory are contained in that module. The cards are either SIMMs (Single In-line Memory Modules,

with 30 or 72 pins) or DIMMs (Dual In-line Memory Modules, with 168 pins). All of the SIMMs or DIMMs in a bank must be the same size.

Most POST routines will first determine the amount of memory present, and check to see that the amount found agrees with the switch settings and CMOS values. Then they will thoroughly test the first 64K, partially test memory above 64K, and test the refresh signal, which is an intermittent voltage supplied to the RAM chips. Some BIOS' will also test each data line and address line individually, which greatly aids troubleshooting. If so, this info will be found in Chapter 3 under the POST code listings for that BIOS. See Appendix A for memory allocations.

Memory may be mapped in different ways from one system to the next. If the system won't boot up because of memory failure and you don't know the mapping strategy in use, the low-tech solution is to get one SIMM or DIMM of the same capacity presently used in the system, and swap out each module in turn until the problem disappears. If the symptoms persist, the problem is most likely with the signals coming to the module: the address lines, data lines, voltages or refresh signal. There is also memory-mapping circuitry on the motherboard which may have failed.

5.2 Protected Mode

The first PCs only had one megabyte of memory, and operated in what is now called Real Mode. Protected mode allows modern operating systems to run in memory above 1 MB. CPUs still have the option to run in Real Mode for backward compatibility, and the POST will switch from one to the other. If this test fails, the culprit is usually the CPU chip or the A-20 Line (see 5.3).

5.3 A-20Line

Address lines A-0 through A-19 access the first megabyte of memory. Address line A-20 is the first line allowing access to extended memory, and must be enabled and disabled as the CPU switches between Real and Protected Mode. Because the 286 CPU did not have circuitry to control this, the IBM engineers routed A-20 through some unused pins on the 8042 Keyboard Controller chip, and it can still be found there

on many systems. On other systems, this function will be found elsewhere on the motherboard. Refer to the documentation to find exactly where. A failure may be indicated as an A-20 test, or as part of the Protected Mode tests.

5.4 ROM

Read-Only Memory will be found on many adapter cards, and on the mother board itself for the BIOS. If a POST code just refers to ROM it almost always means adapter-card ROM. The POST will start at memory address C800:0000 and check in 2K increments for a value of 55AA hex, which indicates a device is using that section of ROM. The POST will then execute the initialization program for the device, starting at the fourth byte of that section.

If the POST stops during the ROM test, you must isolate which device is causing the problem. Starting with the most recently added device, remove the adapter cards one at a time until the problem disappears. It may be a defective I/O device or its adapter card, but often is just a problem with the setup of the device. Common errors are two devices both trying to use the same section of memory, or set to the same IRQ or DMA values.

5.5 ROM Shadowing

Most systems have the ability to move ROM code into RAM, where it can be accessed much faster. If this test fails, disable ROM shadowing in the CMOS, and turn it back on a portion at a time. Start by enabling shadowing for the BIOS ROM, then Video ROM. If the System Setup allows, enable shadowing by the other adapter cards one at a time until the culprit is found. The cure could be either the card's ROM or the RAM for that memory section. As a quick fix, you may be able to just leave shadowing disabled for that device.

5.6 Cache

In 486 and later processors, the CPU has internal cache memory for faster access to frequently needed RAM contents. This is Level 1 Cache, and if it fails, the CPU is defective. Additional cache is provided by static SRAM chips external to the CPU, called Level 2 Cache. Some new CPUs have Level 2 cache in CPU, and call it Unified

Cache. With a Level 2 Cache failure, either the SRAM or CPU is defective, or the system expects external cache but none is installed.

5.7 DMA

Direct Memory Access. Allows data transfers to and from memory without monopolizing the CPU. All systems since the 286 use two cascaded DMA chips to provide 15 DMA channels, or a VLSI chip that combines DMA with the PIT, PIC and RTC functions. You may get a POST code for DMA, but you should also suspect the DMA if RAM fails and can't be fixed by swapping the memory modules.

6.0 I/O

(Input/Output): This covers any devices, which send information to and from the motherboard, except for the video and keyboard, which are covered separately. This includes the floppy and hard drives, and the serial and parallel ports. Most BIOS routines do not test the CD-ROM or sound cards.

6.1 I/O Enable

A few POSTs will test the ability to enable and disable an integrated I/O Controller.

6.2 Serial Ports

The POST will search for serial ports, and then test them. An error shows that a port was found, and that a problem was detected with it. Most systems have serial ports designated COM1 and COM2, and the POST may tell you which was being tested. It may also refer to an RS232 test. Older systems will have serial controllers that can be replaced, but most newer systems have a large-scale integrated I/O controller surface-mounted on the motherboard.

6.3 Parallel Ports

An error indicates that the POST found a parallel port, but it was not functioning properly. The problem is usually the I/O controller. Older systems will have a parallel controller card, but on most newer systems, it will be part of an integrated I/O Controller on the motherboard.

6.4 Hard Drive

The POST will first query the controllers and compare to what the CMOS says should be there. It may then do a seek test of each drive, to the last cylinder and then to the first. The problem may be the drive or the controller, but it could also be the CMOS values. If you can load a diagnostic disk such as Micro-Scope, you can better pin-point the failure area.

6.5 Floppy Drive

The BIOS will initialize and test the floppy drive. As with the hard drive, a failure could be the controller, the drive, or corrupted CMOS.

6.6 Miscellaneous I/O

Many newer BIOS will test the dedicated mouse port, and a few will check for a game port. If the mouse port fails, make sure the mouse is plugged in (and doesn't have the keyboard plugged into that port). The game port may fail because no controller is dedicated to that port, and you will have to disable or remove the port in order to pass the POST. Refer to the system documentation for instructions.

7.0 Video

The POST may interrogate the Video Card to see what kind of monitor is installed. If the test fails, most likely the monitor is not connected or doesn't match CMOS parameters.

7.1 Monochrome Display

The BIOS may separately initialize the monochrome and color control circuitry, as a holdover from the days when color monitors were a novelty. If the controllers are actually separate, they will be found on the motherboard rather than on a video adapter card.

7.2 Color Display

See 7.1, Monochrome Display.

7.3 Video ROM

The POST looks for a value of 55AAh at memory location C000:0000, and will then run the program located at C000:0003. If this test fails, it will probably be a faulty video card, but it could also be that the video card identified in CMOS does not match the one installed in the system.

7.4 Video RAM

The amount of system RAM allotted to video is not enough for today's graphic-intensive programs so video adapters will have their own RAM located on the adapter card itself. If this test fails, replace the video card.

8.0 Keyboard

The POST will see if it can detect the keyboard, and will also test the keyboard controller. If the keyboard is not detected, make sure it is plugged in, and then check the connector. As a last resort, swap out the keyboard, which may be defective or may just need a good cleaning.

8.1 Keyboard Controller

The keyboard controller chip (8042, 8742) is located on the motherboard and controls serial data transfers to and from the keyboard, often including the reset signal to the CPU. The controller uses IRQ1 for keystroke data coming in from the keyboard, and stores the keystrokes in an internal buffer until the interrupt is recognized by the CPU.
Some POST routines run extensive tests of the keyboard functions, but any failure still comes down to replacing either the keyboard or the controller chip.

8.2 A-20 Line

One line of the keyboard controller is often used to control Address line 20. More information on this is available under section 5.2, PROTECTED MODE.

8.3 Keyboard Lock

For security, some systems come with a keyboard lock that prevents the system from accepting keyboard input. This is a physical lock, turned with a key and usually mounted on the front of the case, but sometimes on the keyboard. Only a few BIOS versions test this.

8.4 Turbo Switch

On some systems, POST will check this switch, usually located on the front of the case next to the Reset switch. The switch has no function on 486 or higher CPUs.

9.0 Error Display

If errors occur during the POST, many BIOS versions will attempt to put a message on the monitor screen telling you what failed. If the system is functioning well enough for the message to arrive on the screen, consider yourself lucky. Most of these error messages are self-explanatory, but IBM PC and PS/2 systems send a 6-digit code. These codes are listed at the end of the BIOS codes chapter.

10.0 Reserved

Certain POST codes are marked **Reserved** or **OEM-specific**. The BIOS manufacturer will assign these as requested by their customers, and you will need to contact your system vendor or motherboard manufacturer to find out what function has been assigned to a particular reserved code.

Codes marked **Debug** are used by the manufacturer to test the chips, but are not used during normal POST.

Chapter 3
BIOS POST Code Listings

AMI 2.2 BIOS

Post Code	Diag. Sect.	Description
00	2.2	Flag Test
03	2.2	Register Test
06	2.4	Chipset Test
09	4.2	BIOS Checksum
0C	5.7	Page Register
0F	3.2	8254 Timer
12	3.2	Memory Refresh
15	5.7	DMA Controllers
18	5.7	8237 DMA Initialization
1B	3.1	8259 Initialization
1E	3.2	PIC Chips
21	3.2	Memory Refresh (1st Bank)
24	5.1,5.7	Base 64 Address test
27	5.1	Base 64 Memory test
2A	8.1	8742 Keyboard Chip
2D	2.6	MC146818 RTC/CMOS
30	5.2	Protected Mode
33	5.1	Size Memory
36	5.2	Protected Mode
39	5.2	Protected Mode Failed
3C	2.5	CPU Speed Calculation
3F	8.0	Read 8742 Hardware Switches

AMI 2.2 BIOS Continued		
42	3.1	Initialize Interrupt Vector Area
45	2.6	Verify CMOS Configuration
48	7.0	Test & Initialize Video System
4B	3.1	Unexpected Interrupt Test
4E	5.2	Start 2nd Protected Mode Test
51	8.1	Verify LTD Instruction
54	8.1	Verify TR Instruction
57	8.1	Verify LSL Instruction
5A	8.1	Verify LAR Instruction
5D	8.1	Verify VERR Instruction
60	8.1	Address Line 20 Test
63	8.1	Unexpected Exception Test
66	5.2	Start 3rd Protected Mode Test
69	5.1, 5.7	Address Line Test
6C	5.1	System Memory Test
6F	5.5	Shadow Memory Test
72	5.1	Extended Memory Test
75	2.6	Verify Memory Configuration
78	2.6	Display CMOS Error Messages
7B	4.0, 5.7	Copy System BIOS Shadow Memory
7E	3.2	8254 Clock Test
81	2.5, 2.6	MC146818 RTC Test
84	8.0	Keyboard Test
87	8.0	Determine Keyboard Type
8A	8.0	Stuck Key Test
8D	3.1	Initialize Hardware Interrupt Vector
90	2.3	Math Coprocessor
93	6.2	Determine COM Ports Available
96	6.3	Determine LPT Ports Available

AMI 2.2 BIOS Continued		
99	2.6, 4.0	Initialize BIOS Data Area
9C	6.4, 6.5	Fixed/Floppy Controller Test
9F	6.5	Floppy Disk Test
A2	6.4	Fixed Disk Test
A5	5.4	External ROM Scan
A8	8.3	System Key Lock Test
AE	2.6	F1 Error Message Test
AF	4.1	System Boot Initialization
B1	4.1	Interrupt 19 Boot Loader

AMI Plus BIOS

Post Code	Diag. Sect.	Description
00	4.1	Control To Interrupt 19
01	2.6	NMI Disabled (Bit 7 of I/O Port 70h).
02	2.2	286 Register Test Over
03	4.2	ROM Checksum OK
04	3.1	8259 Initialization OK
05	2.6, 3.1	CMOS Interrupt Disabled
06	3.2	System Timer Counting OK
07	3.2	CH-0 of 8259 Test OK
08	5.7	CH-2 of Delta Count Test OK
09	5.7	CH-1 of Delta Count Test OK
0A	5.7	CH-0 of Delta Test Count OK
0B	5.7	Parity Status Cleared
0C	5.7, 3.2	Refresh & System Time OK
0D	5.7, 3.2	Refresh Link Toggling OK
0E	5.7, 3.2	Refresh Period ON/OFF 50% OK
10	5.1	About to Start 64K Memory

AMI Plus BIOS Continued		
11	5.1	Address Line Test OK
12	5.1	64K Base Memory Test OK
13	5.1, 4.0	Interrupt Vectors Initialized
14	8.1	8042 Keyboard Controller
15	2.6	CMOS Read/Write Test OK
16	2.6	CMOS Checksum/Battery check
17	7.1	Monochrome Mode Set OK
18	7.2	Color Mode Set OK
19	7.3	Video ROM Search
1A	7.3	Optional Video ROM Control OK
1B	7.4	Display Memory Read/Write Test OK
1C	7.4	Alternate Display Memory OK
1D	7.0	Video Retrace Check OK
1E	7.0	Global Byte set for Video OK
1F	7.0, 2.6	Mode Set for Mono/Color OK
20	7.0	Video Test OK
21	7.0	Video Display OK
22	7.0, 2.6	Power On Message Display OK
30	5.1	Virtual Mode Memory Test
31	5.2	Virtual Mode Memory Test Started
32	5.2	Processor in Virtual Mode
33	5.1	Memory Address Line Test
34	5.1	Memory Address Line Test
35	5.1	Memory Below IMB Calculated
36	5.1	Memory Size Computation OK
37	5.1	Memory Test in Progress
38	5.1	Memory Initialization Over below 1MB
39	5.1	Memory Initialization Over above 1MB
3A	5.1	Display Memory Size

AMI Plus BIOS Continued		
3B	5.1	About To Start below 1MB
3C	5.1	Memory below 1MB OK
3D	5.1	Memory above 1MB OK
3E	5.2	About to go to Real Mode
3F	5.2	Shutdown Successful
40	8.1	About to Disable Gate A-20
41	8.1	Gate A-20 Disabled
42	5.7	About to test DMA Controller
4E	2.1	Address Line Test OK
4F	5.2	Processor In Real Mode
50	5.7	DMA Page Register Test OK
51	5.7	DMA Unit-1 Base Register
52	5.7	DMA Unit-1 Channel Register OK
53	5.7	DMA Channel-2 Base register Test OK
54	5.7	About to test Latch for Unit-1
55	5.7	F/F Latch Tests both Units OK
56	5.7	DMA Units 1 & 2 programmed OK
57	3.1	8259 Initialization Over
58	3.1	8259 Mask Register Check OK
59	3.1	Master 8259 Mask Register OK
5A	3.2	Check Timer & Keyboard Interrupt
5B	3.2	Timer Interrupt OK
5C	3.2	About to test Keyboard Interrupt
5D	3.2	ERROR! Timer/Keyboard Interrupt
5E	3.2	8259 Interrupt Controller Error
5F	3.2	8259 Interrupt Controller Test OK
70	8.1	Start of Keyboard Test
71	8.1	Keyboard Bat Test OK
72	8.1	Keyboard Test OK

AMI Plus BIOS Continued		
73	8.1	Keyboard Global Data Initialize
74	6.5	Floppy Setup about to start
75	6.5	Floppy Setup OK
76	6.4	Hard Disk Setup about to start
77	6.4	Hard Disk Setup OK
79	2.6	About to Initialize Timer Data
7A	2.6	Verify CMOS Battery Power
7B	2.6	CMOS Battery Verification Done
7D	5.1	Analyze Test Results for Memory
7E	5.1	CMOS Memory Size Update OK
7F	7.3	Check Optional ROM C000:0
80	8.1	Keyboard Sensed to Enable Setup
81	5.4	Optional ROM Control OK
82	6.3	Printer Global Data Init. OK
83	6.2	RS-232 Global Data Init. OK
84	2.3	80287 Check/Test OK
85	9.0	About to display Soft Error
86	4.0	Give Control to System ROM E000
87	4.0	System ROM E000 Check Over
00		Call to Interrupt 19 for boot loader

AMI Color

Post Code	Diag. Sect.	Description
00	4.1	Control to Int 19 Boot Loader
01	2.2	CPU Test
02	3.2	Power-On Delay
03	2.4	Chipset Initialization
04	8.1	Soft/Hard Reset
05	2.6	ROM Enable

AMI Color Continued		
06	4.2	ROM BIOS Checksum
07	8.1	8042 Test
08	8.1	8042 Test
09	8.1	8042 Test
0A	8.1	8042 Test
0B	8.2	8042 Protected Mode Test
0C	8.1	8042 Test
0D	2.6	8042 Test, CMOS
0E	2.6	CMOS Checksum
0F	2.6	CMOS Initialization
10	2.5, 2.6	CMOS/RTC Status
11	3.1, 5.7	DMA/PIC Disable
12	3.1, 5.7	DMA / PIC Initialization
13	5.1	Chipset/Memory Initialization
14	3.2	8254 Timer Test
15	3.2	CH-2 Timer Test
16	3.2	CH-1 Timer Test
17	3.2	8254 CH-0 Test
18	3.2	Memory Refresh Test
19	3.2	Memory Refresh Test
1A	3.2	Check 15-microsecond Refresh
1B	3.2	Check 30-microsecond Refresh
20	5.1	Base 64K Memory Test
21	5.1	Base Memory Parity Test
22	5.1	Memory Read/Write
23	5.1	BIOS Vector Initialization
24	5.1	BIOS Vector Initialization
25	8.4	Turbo Check of 8042
26	8.4	Global Data Table for Turbo

AMI Color Continued		
27	2.6, 7.0	Video Mode Test
28	7.1	Monochrome Test
29	7.2	Color Test
2A	7.4	Parity Enable Test
2B	7.3	Optional ROM Check Start
2C	7.3	Video ROM Check
2D	2.6	Reinitialize Chipset
2E	7.4	Video Memory Test
2F	7.4	Video Memory Test
30	7.0	Video Adapter Test
31	7.4	Alt. Video Memory Test
32	7.0	Alt. Video Adapter Test
33	7.0	Video Mode Test
34	7.0	Video Mode Set
35	4.0	BIOS ROM Data Area
36	2.6	Power-On Message Display
37	2.6	Power-On Message Display
38	2.6	Read Cursor Position
39	2.6	Display Cursor Reference
3A	2.6	Display Hit <ESC> Message
40	5.2	Protected Mode Start
41	4.0, 5.1	Build Descriptor Tables
42	5.2	Protected Mode Entry
43	3.2, 5.2	Protected Interrupt Enable
44	5.1	Check Descriptor Tables
45	5.1	Size Memory
46	5.1	Memory Read/Write Test
47	5.1	Base 640K Memory Test
48	5.1	640K Memory Size
49	5.1	Extended Memory Size

AMI Color Continued		
4A	5.1	Extended Memory CMOS Verify
4B	8.1	Check for Soft/Hard Reset
4C	5.7	Clear Extended Memory
4D	2.6, 5.1	Update CMOS on Memory Size
4E	2.6, 5.1	Base RAM Displayed
4F	5.1	Memory Read/Write Test on 640K
50	2.6, 5.1	Update CMOS on RAM Size
51	5.1	Extended Memory Test
52	5.1	Re-size Extended Memory
53	5.2	Re-enter Real Mode
54	4.0	Restore CPU Registers
55	5.2	A-20 Gate Disabled
56	3.2, 5.1	BIOS Vector Recheck
57	3.2, 5.1	BIOS Vector Half Checked
58	2.6	Clear Hit <ESC> Message
59	2.4	DMA, PIT Test
60	5.7	DMA Page Register Test
61	5.7	DMA #1 Test
62	5.7	DMA #2 Test
63	3.2, 5.1	BIOS Data Area Check
64	3.2, 5.1	BIOS Data Area Halfway Point
65	5.7	Initialize DMA Chips
66	3.1	8259 Initialization
67	8.1	Keyboard Test
80	8.1	Keyboard Reset
81	8.1	Stuck Key and Batch Test
82	8.1	8042 Reset
83	8.3	Lock Key Check
84	8.3	Compare Memory Size with CMOS
85	2.6	Password/Soft Error Check

AMI Color Continued		
86	2.6	XCMOC/CMOS Equipment Check
87	2.6	CMOS Setup Entered
88	2.4	Reinitialize Chipset
89	2.6	Display Power-On Message
8A	2.6	Display Wait and Mouse Check
8B	2.6	Shadow any Option ROMs
8C	2.6	Initialize XCMOS Settings
8D	6.4, 6.5	Reset Hard/Floppy Drives
8E	2.6, 6.5	Floppy Compare to CMOS
8F	6.5	Floppy Initialization
90	2.6, 6.4	Hard Disk Compare to CMOS
91	6.4	Hard Disk Initialization
92	3.2, 5.1	BIOS Data Table Check
93	3.2, 5.1	BIOS Data Check at halfway
94	2.6, 5.1	Set Memory Size
95	7.0	Verify Display Memory
96	3.2, 5.7	Clear Interrupts
97	7.0	Optional ROM Check
98	3.2, 5.7	Clear Interrupts
99	2.5, 3.2	Setup Timer Data/RS232 Base
9A	6.2	RS232 Test
9B	3.2, 5.7	Clear Interrupts
9C	2.3	NPU Test
9D	3.2, 5.7	Clear Interrupts
9E	8.1	Extended Keyboard Check
9F	8.0	Set Numlock
A0	8.1	Keyboard Reset
A1	5.6	Cache Memory Test
A2	2.6	Display Soft Errors
A3	2.6, 8.0	Set Typematic Rate

AMI Color Continued		
A4	2.6	Memory Wait States
A5	2.6	Clear Screen
A6	2.6, 5.7	Enable Parity/NMI
A7	3.2, 5.7	Clear Interrupts
A8	2.6, 5.1	Control to E000
A9	3.2, 5.7	Clear Interrupts
AA	2.6	Display Configuration
00		Call to Interrupt 19 for boot loader

AMI Ez-Flex BIOS

Post Code	Diag. Sect.	Description
01	2.2	Disable NMI, Start CPU Flag Test
02	1.0	Power-On Delay
03	2.4	Initialize Chipset
04	8.1	Keyboard Hard/Soft Reset
05	5.4	ROM Enable
06	4.2	ROM BIOS Checksum
07	8.1	8042 Keyboard Controller Test
08	8.1	8042 Keyboard Controller Test
09	8.1	8042 Keyboard Controller Test
0A	8.1	8042 Keyboard Controller Test
0B	5.2, 8.2	Test 8042 Protected Mode
0C	8.1	8042 Keyboard Controller Test
0D	2.7	Test CMOS RAM Shutdown Register
0E	2.6	Test CMOS Checksum
0F	2.6	Initialize CMOS
10	2.5, 2.6	CMOS/RTC Status OK
11	3.1, 5.7	Disable DMA and PIC
12	7.0	Disable Video Display

AMI Ez-Flex BIOS Continued		
13	2.4, 5.0	Initialize Chipset and Memory
14	3.1	8254 PIC Tested
15	3.2	PIT Channel 2
16	3.2	PIT Channel 1
17	3.2	PIT Channel 0
18	3.2, 5.0	PIT Memory Refresh
19	3.2, 5.0	PIT Memory Refresh
1A	3.2, 5.0	Check PIT 15 Microsecond Refresh
1B	5.0	Test Base 64K Memory
20	5.0	Test Address Lines
21	5.0	Test Base 64K Parity
22	5.0	Test Memory Read/Write
23	3.0	Setup Prior to Vector Table Initialization
24	3.0	Initialize Vector Table in Lower 1K of RAM
25	8.1	Test 8042 Keyboard Controller
26	8.1	Keyboard Controller Global Function
27	3.0	Setup for Vector Table Initialization
28	7.1	Test Video Monochrome Mode
29	7.2	Test Video Color Mode (CGA)
2A	5.0	Test Parity Enable
2B	5.4	Check for Optional ROMs
2C	7.3	Check for Video ROM
2D	7.2	Check for EGA/VGA
2E	7.4	Test Video Memory (non-EGA/VGA)
2F	7.4	Test Video Memory
30	7.0	Test Video Adapter
31	7.4	Test Alternate Video Memory
32	7.0	Test Alternate Video Adapter
33	7.0	Test Video Mode

AMI Ez-Flex BIOS Continued		
34	7.0	Test Video Mode
35	4.0	Initialize BIOS ROM Area
36	1.0	Set Power-On Display Cursor
37	1.0	Display Power-On Message
38	7.0	Read Cursor Position
39	7.0	Display Cursor Reference
3A	7.0	Display Setup Message
40	5.2	Protected Mode Tested
41	2.7	Build Descriptor Tables
42	5.2	CPU in Protected Mode
43	5.2	Enable Protected Mode Interrupt
44	2.7	Check Descriptor Tables
45	5.0	Check Memory Size
46	5.0	Memory Read/Write Test
47	5.0	Test Base 640KB of RAM
48	5.0	Check for Memory Below 1MB
49	5.0	Check for Memory Above 1MB
4A	4.0, 5.5	Check BIOS ROM Data Area
4B	5.0	RAM Below 1MB Cleared for Soft Reset
4C	5.0	RAM Above 1MB Cleared for Soft Reset
4D	2.6, 5.0	Update CMOS Memory Size
4E	5.0	Display Base 64KB Memory Test
4F	5.0	Test Base 640KB Memory
50	5.0, 5.5	RAM Size Update for Shadowing
51	5.0	Test Extended Memory
52	5.2	System Prepared for Real Mode
53	2.2, 5.2	Return CPU to Real Mode
54	2.2	Return CPU Registers to Real Mode
55	5.3	Disable A-20 Gate

AMI Ez-Flex BIOS Continued		
56	5.5	BIOS Data Area Re-Checked
57	5.5	BIOS Data Area Check Complete
58	7.0	Display Set-up Message
59	5.7	DMA Register Page Test
60	7.4	Verify Display Memory
61	5.7	Test DMA #1
62	5.7	Test DMA #2
63	5.5	BIOS Data Area Check
64	5.5	BIOS Data Area Check Complete
65	5.7	Initialize DMA
66	3.1	Initialize 8259 PIC
67	8.0	Keyboard Test
80	8.0	Keyboard Reset
81	8.0	Stuck Key and Batch Test
82	8.1	Test 8042 Keyboard Controller
83	8.3	Check Lock Key
84	2.6, 5.0	Compare Memory Size to CMOS
85	4.3	Check Password and Soft Error
86	2.6	CMOS Equipment Check
87	2.6	CMOS Setup
88	2.4	Initialize Chipset
89	1.0, 7.0	Display Power-On Message
8A	6.6	Check Mouse and Display Wait Message
8B	5.5	Attempt to Shadow Option ROMs
8C	2.6	Initialize System with CMOS Settings
8D	6.1	Reset Hard Drives and Floppy Drives
8E	2.6, 6.5	Compare Floppy Setup to CMOS Settings
8F	6.5	Initialize Floppy Controller
90	2.6, 6.4	Compare Hard Drive to CMOS Settings
91	6.4	Initialize Hard Drive Controller

AMI Ez-Flex BIOS Continued		
92	2.7, 4.0	Check BIOS Data Table
93	2.7, 4.0	BIOS Data Table Check Complete
94	2.6, 5.0	Set Memory Size
95	7.4	Verify Display Memory
96	3.0	Clear All Interrupts
97	5.4	Check for Optional ROMs
98	3.0	Clear All Interrupts
99	3.1	Timer Data Setup
9A	6.2	Check for Serial Ports
9B	3.0	Clear All Interrupts
9C	2.3	Check Math Co-Processor
9D	3.0	Clear All Interrupts
9E	8.0	Extended Keyboard Check
9F	8.1	Set Numlock on Keyboard
A0	8.0	Keyboard Reset
A1	2.2, 5.0	Test Cache Memory Size
A2	5.0	Display Any Soft Errors
A3	8.0	Set Typematic Rate
A4	5.0	Set Memory Wait States
A5	7.0	Clear Display
A6	3.0, 5.0	Enable Parity and NMI
A7	3.0	Clear All Interrupts
A8	5.4	Give System Control to ROM at E0000
A9	3.0	Clear All Interrupts
AA	2.6, 7.0	Display Configuration
00	4.1	Call Boot Loader Int. 19

AMI Win BIOS

Post Code	Diag. Sect.	Description
00	4.1	Control to Int 19 Boot Loader
01	2.6	Disable NMI
02	8.1	Power-On Delay
03	8.1	Soft Reset Power-On
05	5.6	Disable Cache
06	4.0, 5.1	Uncompressed POST Code
08	2.6	CMOS Checksum
08	2.6	CMOS Initialization
0A	2.6	CMOS Initialization for Date and Time
0B	2.4	Initialization Before Keyboard Batch
0C	8.1	Batch Command to Keyboard Controller
0D	8.1	Verify Batch Command
0E	8.1	Initialize After KB Controller Batch
0F	8.1	Write KB Command Byte
10	8.1	Pin 23/24 Block/Unblock Command
11	8.1	Check For <INS> Key Command
12	2.4	DMA/PIC Disable
13	2.4	Chipset Initialization
14	3.2	8254 Timer Test
19	3.2, 5.1	Memory Refresh Test
1A	3.2, 5.1	Check 15 Micro-Second Refresh
20	5.1	Base 64 Test
23	4.0, 5.1	Set BIOS Stack Before Int. Vector Init.
24	2.2, 5.1	Interrupt Vector Initialization
25	2.7, 8.4	Read Input of 9042 Chip, Clear Password
26	8.4	Initialize Global Data for Turbo Switch
27	2.2, 2.4	Initialize before setting Video Mode
28	2.6	Set Video Mode

AMI Win BIOS Continued		
2A	2.1	Initialize BUS (Sys,Static, Output Dev.)
2B	7.3	Setup before Operational Video Check
2C	7.3	Control to Optional Video ROM
2D	2.3	Proc. after Optional Video ROM Routine
2E	2.3	Display Mem R/W Test if No EGA/VGA
2F	5.1, 7.0	Display Memory R/W Test
30	7.0	Retrace Check
31	5.1, 7.0	Display Alternate Memory R/W Test
32	7.0	Alternate Display Retrace Check
34	7.0	Set Display Mode
37	7.0	Display Power-On Message
38	2.1, 2.4	Init. BUS Types (Input, IPL, Gen Devices)
39	2.4, 7.0	Display BUS Initialization Error Messages
3A	7.0	Display the Hit <DEL> Message
3B	5.2	Virtual Mode Memory Test
40	2.2, 2.4	Prepare Descriptor Tables
42	5.2	Enter Virtual Mode for Memory Test
43	2.7, 3.1	Enable Interrupts for Diagnostic Mode
44	5.1	Initialize Data to Check Mem. Wrap At 0:0
45	5.1, 5.2	Check Mem. Wrap, Find Total RAM
46	5.1	Memory Write Test
47	5.1	640K Base Memory Write Test
48	5.1	Determine Memory Below 1 MB
49	5.1	Determine Memory Above 1 MB
4B	2.6, 8.1	Check for Soft Reset, clear Mem below 1 MB
4C	5.1	Clear Memory Above 1 MB
4D	2.6, 4.0	Save Memory Size
4E	5.1	Display First 64K Memory Size
4F	5.1	Sequential and Random Memory Test
50	2.7, 7.0	Displayed Memory Size

AMI Win BIOS Continued		
51	5.1	Above 1MB Memory Test
52	2.6, 5.1	Save Memory Size Information
53	2.2, 5.2	Enter Real Mode
54	5.2	Disable Gate A-20 Line
57	5.7	Adjust Memory Size
58	8.1	Clear Hit <DEL> Message
59	3.1, 5.7	DMA/PIC Test
60	5.7	DMA #1 Base Register Test
62	5.7	DMA #2 Base Register Test
65	2.7, 5.7	Program DMA Unit 1 and 2
66	3.1	Initialize 8259 Interrupt Controller
67	8.1	Keyboard Test
7F	8.1	Enable Extended NMI Sources
80	8.1	Stuck Key and Batch Test
81	8.1	Keyboard Controller Test
82	8.1	Write Command Byte, Init. Circular Buffer
83	8.3	Lock Key Check
84	2.6	Compare Memory Size with CMOS
85	2.6	Password/Soft Error Check
86	2.6	Programming Before Setup
87	2.6	Execute CMOS Setup
88	2.6	Programming After Setup
89	7.0	Power-On Display
8B	2.7, 7.3	Shadow Main and Video BIOS
8C	2.4	Setup Options After CMOS Setup
8D	2.7, 6.2	Initialize Mouse
8E	6.4	Reset Hard Disk Controller
8F	6.5	Floppy Setup
91	6.4	Hard Disk Setup
94	2.6	Base/Extended Memory Size

AMI Win BIOS Continued		
95	2.1	Init. PCI/VLB BUS Optnl ROMs from C800
96	2.1	Initialize Before C800 Optnl ROM Control
97	5.4	Control to Optional ROM
98	2.4	Processing After Optional ROM Control
99	2.4	Setup Timer Data Area/Printer Base Address
9A	6.2	Set RS-232 Base Address
9B	2.4	Initialize Before NPU Test
9C	2.3	NPU Initialization
9D	2.4	Initialization After NPU Test
9E	8.1	Check Extended KB, KB ID and Num-Lock
9F	8.1	Issue Keyboard ID Command
A0	2.6, 8.1	Reset Keyboard ID Flag
A1	5.6	Cache Memory Test
A2	7.0	Display any Soft Errors
A3	2.7, 8.1	Set the Keyboard Typematic Rate
A4	2.4, 2.7	Program Memory Wait States
A5	2.7, 5.1	Clear Screen, Enable Parity NMI
A7	2.4	Init. Needed Before Control to E000 ROM
A8	5.4	Control to E000 ROM
A9	2.4	Init. Needed After Control to E000 ROM
AA	2.7, 7.0	Display System Configuration
B0	2.7, 4.0	Uncompressed SETUP Code for Hot-Key
B1	5.1	Copy any Code to Specific Area
C2	2.4, 2.7	Disable NMI, Power-On Delay
C5	2.7	Enabel ROM, Disable Cache
C6	4.2	ROM BIOS Checksum
C7	2.7	CMOS Shutdown Register Test
C8	2.6	CMOS Checksum
CA	2.5, 2.6	Initialize CMOS Date and Time
CB	2.4	Initialization Before Keyboard Batch

AMI Win BIOS Continued		
CD	8.1	BAT Command to Keyboard Controller
CE	8.1	Installation After KB Controller Batch
CF	8.1	Write Keyboard Command Byte
D1	8.1	Check for <INS> Key Command
D2	3.1, 5.7	Disable DMA and Interrupt Controllers
D3	2.4, 5.1	Chipset Initialization/Auto Detect Memory
D4	4.0, 5.1	Uncompressed RUNTIME Code
D5	4.0	RUNTIME Code Uncompressed
DD	4.0, 5.1	Control to Shadow RAM at F000:FFF0

AMI Win Boot Block Recovery

Note: These codes should only appear if a malfunction occurs while updating the BIOS flash ROM.

Post Code	Description
E0	Initialize Floppy Controller, Test Base RAM
E1	Initialize Interrupt Vector Table
E2	Initialize Interrupt and DMA Controllers
E6	Enable Floppy, IRQs and Internal Cache
ED	Initialize Floppy Drive
EE	Read First Sector of Drive A
EF	Read Error, Drive A
F0	Search for AMIBOOT.ROM in Root Dir.
F1	AMIBOOT.ROM not found in Root Dir.
F2	Reading FAT to Find AMIBOOT.ROM
F3	Reading AMIBOOT.ROM File
F4	Incorrect Size for AMIBOOT.ROM
F5	Disable Internal Cache
FB	Detecting ROM Type
FC	Erasing Flash ROM
FD	Programming Flash ROM

AMI Win Boot Block Recovery Continued	
FF	Programming Done, Restart BIOS

AMI BIOS 8

Post Code	Diag. Sect.	Description
00	4.1	Control to Int 19 Boot Loader
03	2.6, 3.0	Disable NMI, Initialize CMOS
04	2.6	Verify CMOS Checksum
05	3.1	Initialize PIC and Int Vector Table
06	3.2	Initialize System Timer
08	2.2	Initialize CPU
0A	8.1	Initialize Keyboard Controller
0B	6.x	Detect PS/2 Mouse
0C	8.0	Detect Keyboard
0E	6.6	Init Input Devices, Update Kernel Variables
13	2.4	Initialize Chipset Registers
24	4.0	Start Platform-specific BIOS Modules
2A	2.1, 7.4	Initialize PCI bus and any Video Devices
2C	7.3	Initialize Video Adapter and ROM
2E	6.1	Initialize All Output Devices
30	2.1	Initialize System Management Interrupt
31	6.6	Activate ADM Module
33	7.1	Setup to Display Text Information
37	7.3	Display Sign-on and CPU info
38	2.1	Configures PnP and PCI Devices
39	2.7	Initialize DMAC
3A	2.5	Initialize RTC Date and Time
3B	5.1	Test for Total Memory, Display Total.
3C	2.4	Mid-Post Initialization of Chipset Registers
40	2.3, 6.1	Detect Ports, NPU

AMI BIOS 8 Continued		
50	5.1	Adjust for Memory Holes
52	2.6	Update CMOS Memory Total
60	8.0	Set NumLock and Keyboard Rate
61-70		OEM-specific Errors
75	6.4	Initialize Int 13 (for Disk I/O)
78	4.1	Initializes IPL (Boot) Devices
7A	5.4	Initialize Remaining ROM
7C	2.1	Write PnP Data to RAM
84	9.0	Log POST Errors
85	9.0	Display Errors
87	4.0	Execute BIOS Setup if Needed
8C	2.4	Late-Post Initialization of Chipset Registers
8D	1.0	Build ACPI Tables (if ACPI pwr mgmt supp)
8E	3.0	Set NMI
90	2.1	Init. System Management Interrupt
A0	4.3	Check Boot Password, if Installed
A1	4.1	Cleanup Before Boot to OS
A2	3.0	Initialize IRQ Routing Table
A4	7.1	Initialize Runtime Language Module
A7	2.2	Initialize CPU, Display Sys Config Screen
A8	2.2	Prepare CPU for Boot
A9	9.0	Wait for User Response to Config, if Needed
AA	3.0	Uninstall Int 09 and 1C Vectors
AB	4.1	Prepare BIOS Boot Spec. for Int 19 Boot
AC	2.4	End of Post Initialization of Chipset Registers
B1	1.0	Save Sys Context for ACPI Power Mgmt
C0	2.2, 5.6	Disable Cache, Early CPU Initialization
C1	4.1	Setup Boot Processor Info
C2	4.1	Set Boot Processor for POST
C5		Setup Application Processors

AMI BIOS 8 Continued		
C6	5.6	Re-enable Cache
C7	2.2	Exit Early CPU Initialization

AMI BIOS 8 Boot Block Initialization

Note: These codes will appear while updating the BIOS flash ROM.

Post Code	Description
Before D1	Early Chipset Initialization and Super I/O Initialization Is done. NMI Disabled.
D1	Keyboard Controller Test. Check Power Mgmt Wakeup. Save Power-on CPUID in Scratch CMOS.
D0	Verify Boot block Checksum.
D2	Disable Cache, Size Memory.
D3	Additional Chipset Initialization, Enable Cache
D4	Test Base 512K RAM.
D5	Copy Boot block to RAM.
D6	Test BIOS Checksum, Test Forced BIOS Recovery
D7	Restore CPUID.
D8	Runtime Module Uncompressed into RAM.
D9	Copy Main BIOS Into RAM.
DA	Restore CPUID. Give Control to BIOS POST.
E1-E8 EC-EE	OEM-specific Errors. Reserved for Chipset and System Manufacturers.

AMI BIOS 8 Boot Block Recovery

Note: These codes should only appear if a malfunction occurs while updating the BIOS flash ROM.

Post Code	Description
E0	Initialize Floppy, DMA and PIC

AMI BIOS 8 Boot Block Recovery Continued	
E9	Setup Floppy Controller, Attempt Read
EA	Enable ATAPI, Read from CD-ROM
EB	Disable ATAPI
EF	Read Error
F0	Search for Recovery File in Root Directory
F1	Recovery File Not Found
F2	Analyze FAT to Locate Recovery File Clusters
F3	Read Recovery File, Cluster by Cluster
F5	Disable L1 Cache
FA	Compare Recovery File to Flash ROM
FB	Verify Flash ROM Part.
F4	Recovery File Size Does Not Match Flash Part Size
FC	Erase Flash ROM
FD	Program Flash ROM
FF	Flash Update OK. Disable Flash Write. Restore CPUID.

Award BIOS (original XT)

Post Code	Diag. Sect.	Description
03	2.2, 2.5	Flag Register Test
06	2.2, 2.5	CPU Register Test
09	2.4	System Hardware Initialization
0C	4.2	BIOS Checksum
0F	5.7	DMA Page Register Initialization
12	5.7	Test DMA Address and Count Registers
15	5.7	DMA Initialization
18	3.2	Timer Test
1B	3.2	Timer Initialization
1E	3.2, 5.7	Start RAM Refresh

Award BIOS (original XT) Continued		
21	5.1	Test Base 64K of RAM
24	3.1	Setup Init and Temp Stack
27	3.1	Initialize PIC
2A	3.2	Interrupt Mask Register Test
2D	3.1, 3.2	Hot Interrupt Test
30	2.3, 5.7	V40 DMA if present
33	2.4	Verify System Clock Initialization
36	8.1	Keyboard Test
39	2.4, 5.1	Set up Interrupt Table
3C	2.0	Read System Configuration Switches
3F	7.0	Video Test
42	6.2	Serial Port Determination
45	6.3	Parallel Port Determination
48	6.0	Game Port Determination
4B	7.0	Copyright Message Display
4E	2.5	Calculation of CPU Speed
54	5.1	Test of System Memory
55	6.5	Floppy Drive Test
57	6.4, 6.5	System Initialized Before Boot
5A	4.1	Call to Int 19

Award XT Version 3.1

Post Code	Diag. Sect.	Description
01	2.2, 2.5	Processor Test
02	2.4	Type of POST/Keyboard Buffer
06	2.4	Initialize 6845, 8237, 59, 53
07	2.2	Process Registers
09	4.2	ROM Checksum
0A	7.0	Initialize the Video

Award XT Version 3.1 Continued		
15	5.1	Test First 64K Memory Bank
16	3.1	Set Up Interrupt Tables
17	7.0	Set Up Video
18	7.4	Test Video Memory
19	3.1	8259 Mask Bits-Channel 1
1A	3.1	8259 Mask Bits-Channel 2
1E	5.1	Size Memory
1F	5.1	Test Base Memory
20	3.1	Test Stuck 8259s
21	3.1, 3.2	Test Stuck NMI
22	6.5	Initialize Floppy Drive
2C	6.2	Initialize COM Ports
2D	6.3	Initialize LPT Ports
2F	2.3	Initialize Math Coprocessor
31	5.4	Initialize Option ROMs
FF	4.1	Int. 19 Boot Attempt

Award Version 3.3

Post Code	Diag. Sect.	Description
01-05	8.1	Keyboard Controller
06	2.4	On-board LSI
07	2.2	CPU
08-0E	2.4	CMOS, 8254, 8237, 8259, EPROM
0F	2.7	Extended CMOS
10-14	3.2	Refresh
15	5.1	First 64K RAM
16	4.0	Interrupt Vector Tables
17	7.0	Video Initialization
18	7.0	Video Memory

Award Version 3.3 Continued		
19	3.1	Interrupt Line Mask
1A	3.1	Interrupt Line Mask
1B	2.6	Battery Good
1C	2.6	CMOS Checksum
1D	2.6	CMOS Chip
1E	5.1	Memory Size
1F	2.1, 5.1	Memory Verifier
20-23	2.4	CPU Support Chips
24	5.1	Extended Memory Size
25	5.1	Extended Memory Test
26	5.2	Protected Mode
27	5.5, 5.6	Shadow RAM, Cache controller
28	5.5, 5.6	Shadow RAM, Cache Controller
29	10.0	Reserved
2A	8.1	Initialize Keyboard
2B	6.5	Floppy Drive Initialization
2C	6.2	Serial Port Initialization
2D	6.3	Parallel Port Initialization
2E	6.4	Hard Disk Initialization
2F	2.3	Math Coprocessor
30	10.0	Reserved
31	5.4	Optional ROMs
D0-EF	10.0	Reserved
FF	4.1	Boot

Award EISA

Post Code	Diag. Sect.	Description
01	2.2, 2.5	CPU Flags
02	2.2	CPU Registers

Award EISA Continued		
03	2.4	Initialize DMA, PIC, PIT
04	3.2	Memory Refresh
05	8.1	Keyboard Initialization
06	4.2	ROM Checksum
07	2.6	CMOS, Battery
08	5.1	256K Memory
09	5.6	Cache
0A	2.6, 5.1	Set Interrupt Table
0B	2.6	CMOS Checksum
0C	8.1	Keyboard Initialization
0D	7.0	Video Adapter
0E	7.4	Video Memory
0F	5.7	DMA Channel 0
10	5.7	DMA Channel 1
11	5.7	DMA Page Register
14	3.2	Timer Chip
15	3.1	PIC Controller 1
16	3.1	PIC Controller 0
17	3.1	PIC Stuck Bits
18	3.1	PIC Maskable IRQs
19	3.1	NMI Bit Check
1F	2.7	CMOS XRAM
20	2.6, 5.4	Slot 0
21	2.6, 5.4	Slot 1
22	2.6, 5.4	Slot 2
23	2.6, 5.4	Slot 3
24	2.6, 5.4	Slot 4
25	2.6, 5.4	Slot 5
26	2.6, 5.4	Slot 6
27	2.6, 5.4	Slot 7

Award EISA Continued		
28	2.6, 5.4	Slot 8
29	2.6, 5.4	Slot 9
2A	2.6, 5.4	Slot 10
2B	2.6, 5.4	Slot 11
2C	2.6, 5.4	Slot 12
2D	2.6, 5.4	Slot 13
2E	2.6, 5.4	Slot 14
2F	2.6, 5.4	Slot 15
30	5.1	Memory Size 256K
31	5.1	Memory Test Over 256K
32	2.7	EISA Memory
3C	2.6	CMOS Setup
3D	2.6, 6.2	Mouse/Adapter, CMOS
3E	5.6	Cache RAM
3F	5.4	Shadow RAM
41	6.5	Floppy Drive
42	6.4	Hard Drive
43	6.2	RS232 Parallel
45	2.3	NPU
47	2.6	Speed
4E	2.0	Manufacturing Loop
4F	4.3	Security
50	2.6	CMOS Update
51	2.4	Enable NMI, Cache
52	5.4	Adapter ROMs
53	2.5, 2.6	Set Time
60	5.1	Virus Protection Setup
61	5.6	Boot Speed
62	8.1	Num Lock Setup
63	4.1	Boot

Award EISA Continued		
B0	5.2	NMI In Protected
B1	3.2	Disable NMI
BE	2.4	Chipset Default Initialization
BF	2.4	Chipset Program
C0	5.6	Cache On/Off
C1	5.1	Memory Size
C2	5.1	Base 256K Test
C3	5.1	DRAM Page Select
C4	2.6, 7.0	Video Switch
C5	2.7, 5.5	Shadow RAM
C6	2.6, 5.6	Cache Program
C8	2.4	Speed Switch
C9	2.7, 5.5	Shadow RAM
CA	2.4	OEM Chipset
FF	4.1	Boot

Award PnP BIOS

Post Code	Diag. Sect.	Description
03	4.0, 5.1	Initialize EISA Registers
05	8.1	Keyboard Controller Self-Test
07	2.6	Verify CMOS R/W
09	2.4	OEM Specific Initialization
0A	2.2	Issue CPU ID Instruction
0B	2.4, 5.1	PnP Initialization
0C	2.6, 5.1	Initialization of BIOS Data Area
0D	2.4, 5.1	Program Some of Chipset's Value
0E	2.4	Initialize APIC (Multi-processor BIOS Only)
0F	5.7	DMA Channel 0 Test
10	5.7	DMA Channel 1 Test

Award PnP BIOS Continued		
11	5.7	DMA Page Registers Test
14	3.2	Test 8254 0 Counter 2
15	3.1	Test 8259 Interrupt Mask Bit For Channel 1
16	3.1	Test 8259 Interrupt Mask Bit For Channel 1
19	3.1	Test 8259 Functionality
1E	5.4	If An EISA NVM
30	5.1	Get Size of Base and Extended Memory
31	5.1	Test Base and Extended Memory
32	2.6, 4.0	Test All On-Board Super I/O Ports
3C	2.6, 4.0	Set Flag to allow CMOS Setup Utility
3D	8.1	Install PS2 Mouse
3E	2.4, 5.6	Try To Turn On Level 2
41	6.5	Initialize Floppy Controller
42	6.4	Initialize Hard Drive Controller
43	6.2, 6.3	Initialize Serial & Parallel Ports
45	2.3	Initialize Math Coprocessor
4E	2.6	Show all Error Messages On Screen
4F	2.6	Ask For Password, if needed
50	2.6, 5.1	Write all CMOS Values currently In BIOS
52	5.4	Initialize all ISA ROMs
53	2.5, 5.1	If not PnP BIOS, Initialize Ports
60	5.1	Set Up Virus Protection
61	2.6, 5.6	Try to turn on Level 2 Cache
62	8.1	Program Num Lock & Typematic Speed
63	4.1	Boot System via Int 19h
B0	2.4, 5.2	Unexpected Interrupt in Protected Mode
B1	2.4	Unclaimed NMI occurred
BE	2.6	Program Defaults into Chipset
BF	2.4	Program remaining Chipset Values
C0	2.4	Init. all Standard Devices with Defaults

Award PnP BIOS Continued		
C1	5.1, 5.6	Auto-detect On-Board DRAM & Cache
C3	5.1	Test First 26K DRAM
C5	4.0, 5.1	Copy ROM BIOS to E000-FFFF
FF	4.1	System Booting

Award Elite (Version 4.51 PG)

Post Code	Diag. Sect.	Description
01	2.2	Processor Test 1
02	2.2	Processor Test 2
03	2.4	Initialize Chipset
04	3.2, 5.1	Test Memory Refresh Toggle
05	7.0, 8.1	Blank Video, Initialize Keyboard
07	2.6	Test CMOS Interface and Battery
08	5.1	Set Up Low Memory
09	2.2, 5.6	Early Cache Initialization
0A	5.1	Set Up Interrupt Vector Table
0B	2.6	Test CMOS RAM Checksum
0C	8.1	Initialize Keyboard
0D	7.0	Initialize Video Interface
0E	7.4	Test Video Memory
0F	5.7	Test DMA Controller 0
10	5.7	Test DMA Controller 1
11	5.7	Test DMA Page Registers
14	3.2	Test Timer Counter 2
15	3.1	Test 8259-1 Mask Bits
16	3.1	Test 8259-2 Mask Bits
17	3.1	Test Stuck 8259 Interrupt Bits
18	3.1	Test 8259 Interrupt Functionality
19	3.1	Test Stuck NMI Bits (Parity I/O Check)

Award Elite (Version 4.51 PG) Continued		
1A	2.2, 2.5	Benchmark
1F	2.7	Set EISA Mode
20-2F	2.4, 5.4	Enable Slots 0-15
30	5.1	Size Base and Extended Memory
31	5.1	Test Base and Extended Memory
32	2.7	Test EISA Extended Memory
3C	2.6	Setup Enabled
3D	6.2	Initialize and Install Mouse
3E	5.6	Set Up Cache Controller
41	6.5	Initialize Floppy
42	6.4	Initialize Hard Drive
43	6.2, 6.3	Detect & Init. Serial & Parallel Ports
45	2.3	Detect & Init. Math Coprocessor
4E	2.0	Mfg. POST Loop, or Display Messages
4F	4.3	Security Check
50	2.6	Write CMOS
51	2.4	Pre-Boot Enable
52	5.4	Initialize Option ROMs
53	2.5, 2.6	Initialize Time Value
60	5.1	Set Up Virus Protect
61	5.6	Set Boot Speed
62	8.1	Set Up NumLock
63	4.1	Boot Attempt
B0	8.1	Spurious
B1	3.2	Unclaimed NMI
BE	2.4	Chipset Default Initialization
BF	2.4	Chipset Initialization
C0	2.4, 5.6	Turn Off Chipset Cache
C1	5.1	Memory Presence Test
C5	5.5	Early Shadow

Award Elite (Version 4.51 PG) Continued		
C6	5.6	Cache Presence Test
E1-F	5.1	Setup pages. E-1 = page1, E-2 = page 2, etc
FF	4.1	Boot

Award BIOS Version 6.0

Same as Phoenix Medallion BIOS

Post Code	Diag. Sect.	Description
01	5.5	Expand x-group codes in RAM at 1000:0. *(Note: 01 is the 7th step of POST, not the 1st. It follows C, C0, C1, C3 and C5 in that order.)*
02	10.0	Reserved
03	2.0	Initialize Superio_Early_Init Switch
04	10.0	Reserved
05	2.6	Clear CMOS Error Flag, Blank Out Screen
06	10.0	Reserved
07	8.1	Clear 8042 Interface, Start 8042 Self-Test
08	8.1	Test Super I/O Keyboard Controller
09	10.0	Reserved
0A	6.6, 8.0	Detect Keyboard and Mouse Ports
0B	10.0	Reserved
0C	10.0	Reserved
0D	10.0	Reserved
0E	5.5	Test Shadowing Capability
0F	10.0	Reserved
10	2.4	Auto-Detect for DMI Support
11	10.0	Reserved
12	2.6	Test CMOS Memory, Set RTC Status
13	10.0	Reserved
14	2.4	Set Chipset Default Values
15	10.0	Reserved

Award BIOS Version 6.0 Continued		
16	2.0	Set Early_Init_Onboard_Generator Switch
17	10.0	Reserved
18	2.2	Detect CPU Data
19	10.0	Reserved
1A	10.0	Reserved
1B	3.0	Initialize IRQ Vector Table
1C	10.0	Reserved
1D	2.6	Set Early_PM_Init Switch
1E	10.0	Reserved
1F	8.0	Load Keyboard Matrix (Notebook Only)
20	10.0	Reserved
21	1.0	Initialize HPM (Notebook Only)
22	10.0	Reserved
23	2.6	Load CMOS Settings into BIOS Stack
24	10.0	Reserved
25	10.0	Reserved
26	10.0	Reserved
27	3.1	Initialize Int. 9 Buffer
28	10.0	Reserved
29	2.2, 2.4	Initialize CPU and Chipset
2A	10.0	Reserved
2B	10.0	Reserved
2C	10.0	Reserved
2D	7.0	Display BIOS and CPU Info Onscreen
2E	10.0	Reserved
2F	10.0	Reserved
30	10.0	Reserved
31	10.0	Reserved
32	10.0	Reserved
33	8.0	Reset Keyboard

Award BIOS Version 6.0 Continued		
34	10.0	Reserved
35	10.0	Reserved
36	10.0	Reserved
37	10.0	Reserved
38	10.0	Reserved
39	10.0	Reserved
3A	10.0	Reserved
3B	10.0	Reserved
3C	3.2	Test 8254 PIT Chip
3D	10.0	Reserved
3E	3.1	Test 8259 PIC Channel 1 Bits
3F	10.0	Reserved
40	3.1	Test PIC Channel 2 Bits
41	10.0	Reserved
42	10.0	Reserved
43	3.1	Test PIC Functionality
44	10.0	Reserved
45	10.0	Reserved
46	10.0	Reserved
47	2.1	Initialize EISA Slot
48	10.0	Reserved
49	5.0	Calculate Memory Size
4A	10.0	Reserved
4B	10.0	Reserved
4C	10.0	Reserved
4D	10.0	Reserved
4E	2.2	Initialize CPU and Cache
4F	10.0	Reserved
50	6.6	Initialize USB
51	10.0	Reserved

Award BIOS Version 6.0 Continued		
52	5.0	Test Extended Memory
53	10.0	Reserved
54	10.0	Reserved
55	2.2	Display Number of Processors
56	10.0	Reserved
57	2.1	PNP Initialization
58	10.0	Reserved
59	2.7	Initialize Anti-Virus
5A	10.0	Reserved
5B	7.0	Optional Display Message
5C	10.0	Reserved
5D	6.6	Initialize Super I/O and Audio Switch
5E	10.0	Reserved
5F	10.0	Reserved
60	2.7	OK to Enter Setup Utility
61	10.0	Reserved
62	10.0	Reserved
63	10.0	Reserved
64	10.0	Reserved
65	6.6	Initialize PS/2 Mouse
66	10.0	Reserved
67	3.0, 5.0	Setup Memory Size Interrupt 15h
68	10.0	Reserved
69	2.2, 5.0	Turn On L2 Cache
6A	10.0	Reserved
6B	2.4	Program Chipset Registers
6C	10.0	Reserved
6D	2.1	Assign Resources to ISA PNP Devices
6E	10.0	Reserved
6F	6.5	Initialize Floppy Controller

Award BIOS Version 6.0 Continued		
70	10.0	Reserved
71	10.0	Reserved
72	10.0	Reserved
73	4.0	Test for AWDFLASH.EXE
74	10.0	Reserved
75	6.4	Detect/Install IDE Devices
76	10.0	Reserved
77	6.2, 6.3	Detect Serial and Parallel Ports
78	10.0	Reserved
79	10.0	Reserved
7A	2.3	Initialize Coprocessor
7B	10.0	Reserved
7C	10.0	Reserved
7D	10.0	Reserved
7E	10.0	Reserved
7F	7.1	Switch to Text mode
80	10.0	Reserved
81	10.0	Reserved
82	1.0, 4.3	Enable Power Mgt, Check for Password
83	2.6	Save Stack Data to CMOS
84	2.1, 5.4	Initialize ISA PNP Boot Devices
85	3.0	Assign IRQs to PCI Devices
86	10.0	Reserved
87	10.0	Reserved
88	10.0	Reserved
89	10.0	Reserved
90	10.0	Reserved
91	10.0	Reserved
92	10.0	Reserved
93	4.1	Read Boot Sector for Antivirus Code

Award BIOS Version 6.0 Continued		
94	2.2, 5.0	Final Initialization, Enable L2 cache
95	2.5, 8.0	Update Keyboard and Daylight Savings
96	2.5	Load RTC Date/Time into DOS Tick Timer
C0	2.4	Early Chipset Initialization. This and next four codes actually occur at the beginning of POST, in order of CF, C0, C1, C3 and C5.
C1	2.2, 5.0	Detect Memory and Cache
C3	5.5	Decompress BIOS Code into DRAM
C5	5.5	Shadow BIOS
CF	2.6	Test CMOS Red/Write Functions
FF	4.1	Boot Attempt

Award 6.0 Quick POST

These codes will appear if the Quick Boot option is set in CMOS. This option does a shorter version of POST and is recommended for day-to-day operation but not if there are hardware problems.

Post Code	Diag. Sect.	Description
65	2.4, 6.6, 8.1	Initialize Onboard Devices and Keyboard Controller, Reset Chipset Registers
66	2.2, 3.0, 5.0,	Check CPUID. Initialize Cache and Interrupt Vectors
67	2.6, 8.0	Verify CMOS and Battery. Initialize Keyboard and BIOS Data Area
68	7.4	Initialize Video Adapter, Test Video RAM
69	3.0	Initialize 8259 Channel 1, Mask IRQ 9
6A	5.0	Quick Memory Test
6B	2.1, 2.2, 6.1,	Detect CPU Speed, Initialize Onboard Super I/O, Display PnP Data and Vendor-specific text. Setup Virus Protection.

Award 6.0 Quick POST Continued		
6C-6F		Reserved
70	1.0, 3.0	Initialize Mouse and ACPI Subsystem, Install Interrupt Vectors, Display Setup Message
71	5.0	Initialize Cache Controller
72	6.5	Initialize Floppy Controller and Drives
74	2.3	Initialize NPU
75	6.4	Test Hard Drive Write Protection
76		Reserved
77	4.3, 9.0	Display POST Errors, Check Password
78	2.6, 5.4	Write CMOS Values to RAM, Enable Parity, Initialize Option ROMs
79-7C		Reserved
7D	6.4	Boot Partition Head/Cylinder Values to RAM
7E	4.1	Final Initialization
7F	8.1	Set NumLock Status and System Speed
80	3.0	Set Low Stack, call Int 19h
FF	4.1	Boot

Award 6.0 Boot Block

Used when updating Flash BIOS ROM

Post Code	Description
01	Clear Base Memory
05	Initialize Keyboard Controller
12	Initialize Interrupt Vectors
0D	Initialize Video
41	Initialize Floppy and Onboard Super I/O
FF	Load Boot Sector

COMPAQ General

Post Code	Diag. Sect.	Description
00	2.2	Initialize Flags, MSW, IDTLIN
01	2.0	Read Manufacturing Jumper
02	8.1	8042 received Read Command
03	8.1	No response From 8042
04	5.4	Look for ROM at E000
05	5.4	Look for ROM at C800
06	2.6, 8.1	Normal CMOS Reset Code
08	3.1	Initialize 8259, 80287
09	2.6	Reset Code in CMOS Byte
0A	8.1,8.2	Vector Vis 40:67 Reset Function
0B	8.1, 8.2	Vector Vis 40:67 With E01 Function
0C	2.6, 8.1	Boot Reset Function
0D	3.2	Test #2 8254 Counter 0
0E	3.2	Test #2 8254 Counter 2
0F	8.1	Warm Boot
10	3.2	PPI Disabled, PITs 0 and 1
11	7.0	Initialize (blast) VDU Controller
12	7.0	Clear Screen; Turn ON Video
13	3.2	Test Time 0
14	3.2	Disable RTC Interrupts
15	2.6	Check Battery Power
16	2.6	Battery Has Lost Power
17	2.6	Clear CMOS Diags.
18	5.1	Test Base Memory (First 128k)
19	5.1	Initialize Base Memory
1A	7.0	Initialize VDU Adapters
1B	4.0	The System ROM
1C	2.6	CMOS Checksum

COMPAQ General Continued		
1D	5.7	DMA Controller/Page Registers
1E	8.1	Test Keyboard Controller
1F	5.25.	Test 286 Protected Mode
20	5.1	Test Real and Extended Memory
21	2.5	Initialize Time-of-Day
22	2.33	Initialize 287 Coprocessor
23	8.1	Test the Keyboard and 8042
24	2.5, 8.2	Reset A20, Set Default CPU Speed
25	6.5	Test Diskette Subsystem
26	6.4	Test Fixed Disk Subsystem
27	6.3	Initialize Parallel Printer
28	5.4	Perform Search for Optional ROMs
29	2.6, 5.4	Test Valid System Configuration
2A	7.0	Clear Screen
2B	2.5	Check for Invalid Time and Date
2C	5.4	Optional ROM Search
2D	3.2	Test Timer 2
2F	2.6	Write to Diag. Byte
30	5.1	Clear First 128k Bytes of RAM
31	3.1, 4.0	Load Interrupt Vectors 70-77
32	3.1, 4.0	Load Interrupt Vectors 00-1F
33	2.6	Initialize MEMSIZE and RESETWD
34	2.6	Verify CMOS Checksum
35	2.6	CMOS Checksum is Not Valid
36	2.6	Check Battery Power
37	5.4	Check for Game Adapters
38	6.2	Check for Serial Ports
39	6.3	Check for Parallel Printer Ports
3A	5.4, 8.1	Initialize Port and Comm Time-outs
3B	8.1	Flush Keyboard Buffer

COMPAQ General Continued		
40	8.1	Save RESETWD Value
41	5.1	Check RAM Refresh
42	5.1	Start Write of 128k RAM Test
43	5.1	Reset Parity Checks
44	5.1	Start Verify of 128k RAM Test
45	5.1	Check for Parity Errors
46	5.1	NO RAM Errors
47	5.1	RAM Error Detected
50	2.6	Check for Dual Frequency in CMOS
51	2.6, 7.0	Check CMOS VDU Configuration
52	7.3	Start VDU ROM Search
53	7.3	Vector to VDU Option ROMs
54	7.0	Initialize First Display Adapter
55	7.0	Initialize Second Display Adapter
56	7.0	No Display Adapters Installed
57	7.0	Initialize Primary VDU Mode
58	7.0	Start of VDU Test (Each Adapter)
59	7.0	Check Existence of Adapter
5A	7.0	Check VDU Registers
5B	7.0	Start Screen Memory Test
5C	7.0	End Test of Adapter, Clear Memory
5D	2.6, 7.0	Error Detected on an Adapter
5E	7.0	Test The Next Adapter
5F	7.0	All Adapters Successfully Tested
60	5.1	Start Of Memory Tests
61	5.2	Enter Protected Mode
62	5.1	Start Memory Sizing
63	2.6, 5.1	Get CMOS Size
64	5.1	Start Test of Real Memory
65	5.1	Start Test of Extended Memory

COMPAQ General Continued		
66	5.1	Save Size Memory (Base, Ext.)
67	2.7	128K-Option Installed CMOS Bit
68	5.2	Prepare to Return to Real Mode
69	5.2	Back in Real Mode - Successful
6A	5.2	Protected Mode Error during test
6B	2.7	Display Error Message
6C	5.1	End of Memory Test
6D	2.7	Initialize KB OK String
6E	5.1	Determine Size to Test
6F	5.1	Start MEMTEST
70	5.1	Display XXXXXKB OK
71	5.1	Test Each RAM Segment
72	5.1	High Order Address Test
73	5.1	Exit MEMTEST
74	5.1	Parity Error on Bus
75	5.2	Start Protected Mode Test
76	5.2	Prepare to Enter Protected Mode
77	2.6, 8.1	Test Software Exceptions
78	5.2	Prepare to Return to Real Mode
79	5.2	Back in Real Mode - Successful
7A	5.2	Back in Real Mode - Error Occurred
7B	5.2	Exit Protected Test
7C	5.1	High Order Address Test Failure
7D	5.6	Entered Cache Controller Test
7E	5.6	Programming Memory Cache
7F	4.0, 5.1	Copy System ROM to High RAM
80	8.1	Start of 8042 Test
81	8.1	Do 8042 Self Test
82	8.1	Check Result Received
83	8.1	Error Result

COMPAQ General Continued		
84	8.1	OK 8042, Init Mode = 5D
86	8.1	Start Test, Reset Keyboard
87	8.1	Got Acknowledge, Read Result
88	8.1	Got Result, Check it
89	8.1	Test For Stuck Keys
8B	8.1	Test Keyboard Interface
8A	8.1	Key Seems to be Stuck
8C	8.1	Got Result, Check it
8D	8.1	End of Test, No Errors
90	2.6	Start of CMOS Test
91	2.6	CMOS Seems to be OK
92	2.6	Error on CMOS Read/Write Test
93	5.7	Start of DMA Controller Test
94	5.7	Page Registers Seem to be OK
95	5.7	DMA Controller is OK
96	5.7	8237 Initialization is Complete
97	5.6	Start of NCA RAM Test
A0	6.5	Start of Diskette Tests
A1	6.5	FDC Reset Active (3F2h Bit 2)
A2	6.5	FDC Reset Inactive (3F2h Bit 2)
A3	6.5	FDC Motor ON
A4	6.5	FDC time-out Error
A5	6.5	FDC Failed Reset
A6	6.5	FDC Passed Reset
A8	6.5	Start to Determine Drive Type
A9	6.5	Seek Operation Initiated
AA	6.5	Waiting for FDC Seek Status
AF	6.5	Diskette Tests Complete
B0	6.4	Start of Fixed Drive Tests
B1	6.4	Combo Board Not Found - Exit

COMPAQ General Continued		
B2	6.4	Combo Controller Failed - Exit
B3	6.4	Testing Drive 1
B4	6.4	Testing Drive 2
B5	6.4	Drive Error (Error Condition)
B6	6.4	Drive Failed (Failed to Respond)
B7	6.4	No Fixed Drives - Exit
B8	6.4	Fixed Drive Tests Complete
B9	4.1	Attempt to Boot Diskette
BA	4.1	Attempt to Boot Fixed Drive
BB	4.1	Boot Attempt Failed FD/HD
BC	4.1	Jump to Boot Record
BD	4.1	Drive Error, Retry Booting
BE	2.3	Weitek Coprocessor Test
D0	5.1	Entry to Clear Memory Routine
D1	5.2	Ready to go to Protected Mode
D2	5.1	Ready to Clear Extended Memory
D3	5.2	Ready to Reset Back to Real Mode
D4	5.2	Back in Real Mode
D5	5.1	Clear Base Memory
DD	5.2	Built-in Self-Test Failed
E0	5.5	Ready to Replace E000 ROM
E1	5.5	Completed E000 ROM Replacement
E2	5.5	Ready to Replace EGA ROM
E3	5.5	Completed EGA ROM Replacement

DELL BIOS

Post Code	Diag. Sect.	Description
01	2.2	CPU Register Test
02	2.6	CMOS Write/Read Test

DELL BIOS Continued		
03	4.2	ROM BIOS Checksum
04	3.2	PIT Test
05	5.7	DMA Initialization
06	5.7	DMA page Register
08	5.1	RAM Refresh Verification
09	5.1	First 64k RAM Test
0A	5.1	First 64k RAM Data Line
0B	5.1	First 64k RAM Parity
0C	5.1	Address Line First 64k RAM
0D	5.1	Parity Bad First 64K RAM
10	5.1	Bit 0 First 64K RAM Bad
11	5.1	Bit 1 First 64K RAM Bad
12	5.1	Bit 2 First 64K RAM Bad
13	5.1	Bit 3 First 64K RAM Bad
14	5.1	Bit 4 First 64K RAM Bad
15	5.1	Bit 5 First 64K RAM Bad
16	5.1	Bit 6 First 64K RAM Bad
17	5.1	Bit 7 First 64K RAM Bad
18	5.1	Bit 8 First 64K RAM Bad
19	5.1	Bit 9 First 64K RAM Bad
1A	5.1	Bit 10 First 64K RAM Bad
1B	5.1	Bit 11 First 64K RAM Bad
1C	5.1	Bit 12 First 64K RAM Bad
1D	5.1	Bit 13 First 64K RAM Bad
1E	5.1	Bit 14 First 64K RAM Bad
1F	5.1	Bit 15 First 64K RAM Bad
20	5.7	Slave DMA Register Bad
21	5.7	Master DMA Register Bad
22	3.1	Master PIC Register Bad
23	3.1	Slave PIC Register Bad

DELL BIOS Continued		
25	3.1, 5.4	Interrupt Vector Loading
27	8.1	Keyboard Controller Test
28	2.6	CMOS Power And Checksum
29	2.6	CMOS Validation
2B	7.0	Screen Initialization Bad
2C	7.0	Screen Retrace Test Bad
2D	7.3	Search For Video ROM
2E	7.3	Screen Video ROM
30	7.0	Screen Operable
30	7.0	Screen Running With ROM
31	7.1	Monochrome Monitor Operable
32	7.2	Color (40 Column) Operable
33	7.2	Color (80 Column) Operable
34	2.6, 3.2	Timer Tick Interrupt Test
35	2.6, 8.1	Shutdown Test
36	5.2	Gate A20 Bad
37	8.1	Unexpected Interrupt
38	5.1	Extended RAM Test
3A	3.2	Interval Timer Channel 2
3B	2.5	Time-Of-Day Clock
3C	6.2	Serial Port Test
3D	6.3	Parallel Port Test
3E	2.3	Math Coprocessor Test
41	2.0	System Board Select Bad
42	2.7	Extended CMOS RAM Bad

HP Pavillion Series 3100 & 8000 PCs

Post Code	Diag. Sect.	Description
02	2.2	Verify Real Mode

HP Pavillion Series 3100 & 8000 PCs Continued		
03	3.1	Disable NMI
04	2.2	Get Processor Type
06	2.4	Initialize System Hardware
08	2.4	Initialize Chipset With POST Values
09	2.4	Set IN-POST Flag
0A	2.2, 2.4	Initialize CPU Registers
0B	2.2	Enable CPU Cache
0C	5.6	Initialize Cache to POST Values
0E	2.1	Initialize I/O Component
0F	2.1	Initialize Local IDE BUS
10	2.4	Initialize Power Management
11	2.4	Load Alternate Registers
12	2.2, 5.1	Restore CPU Ctrl Word During Warm Boot
13	2.4	Initialize PCI BUS Mastering Devices
14	8.1	Initialize Keyboard Controller
16	4.2	BIOS ROM Checksum
17	5.6	Initialize Cache Before Mem Size
18	3.2	Initialize 8254 Timer
1A	5.7	Initialize 8237 DMA Controller
1C	3.1	Reset PIC
20	3.2, 5.1	Test DRAM Refresh
22	8.1	Test 8742 Keyboard Controller
24	2.4	Set ES Segment Register to 4 GB
26	5.3	Enable A-20 Line
28	5.1	Autosize DRAM
29	5.1	Initialize POST Mem Manager
2A	5.1	Clear 512K Base RAM
2C	5.1, 5.7	RAM Address Line Failure
2E	5.1	RAM Data Failure, Low Byte
2F	5.6	Enable Cache Before BIOS Shadow

HP Pavillion Series 3100 & 8000 PCs Continued		
30	5.1	RAM Data Failure, High Byte
32	2.5, 2.7	Test CPU, BUS Clock Frequency
33	4.0	Initialize POST Dispatch Manager
34	2.6	Test CMOS RAM
35	2.4	Initialize Alternate Chipset Registers
36	2.4, 4.0	Warm-Start Shut-Down
37	2.4, 2.7	Re-Initialize Chipset (MB Only)
38	5.5	Shadow System BIOS ROM
39	2.7, 5.6	Re-Initialize Cache (MB Only)
3A	5.6	Autosize Cache
3C	2.4, 2.7	Configure Advanced Chipset Registers
3D	2.4, 2.7	Load Alt. Registers New CMOS Values
40	2.4, 2.7	Set Initial CPU Speed
42	2.7, 5.1	Initialize Interrupts
44	2.7, 5.1	Initialize BIOS Interrupts
45	2.7	POST Device Initialization
46	4.0	Check ROM Copyright Notice
47	2.1	Initialize Manager for PCI Option ROMs
48	2.7, 7.0	Check Video Config Against CMOS
49	2.1, 5.4	Initialize Manager for PCI Option ROMs
4A	2.7, 7.0	Initialize all Video Adapters
4B	7.0	Display Quiet Boot Screen
4C	5.5, 7.0	Shadow Video BIOS
4E	7.0	Display BIOS Copyright Notice
50	7.0	Display CPU Type & Speed
51	2.4, 2.7	Initialize
52	8.1	Test Keyboard
54	2.7, 8.1	Set Key Click if enabled
56	2.7, 8.1	Enable Keyboard
58	5.1, 5.4	Test for Unexpected Interrupts

HP Pavillion Series 3100 & 8000 PCs Continued		
59	5.1, 5.4	Initialize POST Display Service
5A	2.4, 5.1	Display "Press F2 To Enter Setup"
5B	2.2, 2.7	Disable CPU Cache
5C	5.1	Test RAM, 512-640K
60	5.1	Test Extended Memory
62	5.1	Test Extended Mem Address Lines
64	2.7	Jump to User Patch 1
66	2.2, 2.7	Configure Advanced Cache Registers
67	2.2, 2.7	Initialize Multi-processor APIC
68	5.6	Enable External & Processor Caches
69	2.7	Set Up SMM Area
6A	5.1	Display External L2 Cache Size
6C	5.1, 7.0	Display Shadow Area Message
6E	5.1	Display High Address for UMB Recovery
70	2.7	Display Error Message
72	2.7	Check for Configuration Errors
74	2.5	Test Real-Time Clock
76	2.7, 8.1	Check for Keyboard Errors
7A	8.3	Test for Key-Lock On
7C	2.4, 5.4	Set Up Hardware Interrupt Vectors
7E	2.3, 2.6	Initialize Co-Processor, if present
80	6.1	Disable On-Board Super I/O Ports
81	5.4	Late POST Device Initialization
82	6.2	Detect & Install External RS232 Ports
83	6.4	Configure Non-MDC IDE Controllers
84	6.3	Detect & install External Parallel Ports
85	2.4, 5.5	Initialize PnP ISA Devices
86	6.1	Re-Initialize On-Board I/O Ports
87	2.0, 2.7	Configure Motherboard Configurable Devices
88	5.1	Initialize BIOS Data Area

HP Pavillion Series 3100 & 8000 PCs Continued		
89	3.1	Enable NMIs
8A	5.1	Initialize Extended BIOS Data Area
8B	6.2	Test & Initialize PS/2 Mouse
8C	6.5	Initialize Floppy Controller
8F	6.4	Determine number of ATA Drives
90	6.4	Initialize Hard Disk Controllers
91	6.4	Initialize Local-BUS HD Controllers
92	2.7	Jump to User Patch 2
93	2.4, 2.7	Build MPTABLE For Multi-processor Boards
94	5.3	Disable A-20 Line
95	2.6, 6.4	Install CD-ROM for Boot
96	2.2, 2.7	Clear Huge ES Segment Register
97	2.4	Fix Up Multiprocessor table
98	5.4	Search for Option ROMs
99	6.4	Check for Smart Drive
9A	5.5	Shadow ROM Option
9C	2.4	Set Up Power Management
9E	2.4	Enable Hardware Interrupts
9F	6.4	Determine Number of ATA & SCSI Drives
A0	2.6	Set Time of Day
A2	8.3	Check Key Lock
A4	2.6, 8.1	Initialize Typematic Rate
A8	7.0	Erase F2 Prompt
AA	8.1	Scan for F2 Keystroke
AC	2.6	Enter SETUP
AE	2.6	Clear IN-POST Flag
B0	2.6	Check For Errors
B2	4.0	POST Done, Prepare To Boot
B4	2.4	One Short Beep Before Boot
B5	2.6, 4.0	Terminate Quiet Boot

HP Pavillion Series 3100 & 8000 PCs Continued		
B6	4.3	Check Password (Optional)
B8	2.2, 2.7	Clear Global Descriptor Table
B9	7.0	Clean up all Graphics
BA	2.4	Initialize DMI Parameters
BB	2.4	Initialize PnP Option ROMs
BC	2.6	Clear Parity Checkers
BD	2.7	Display Mullet Boot Menu
BE	7.0	Clear Screen Optional
BF	2.7	Check Virus & Back-Up Reminders
C0	4.1	Try to Boot with Int 19
C1	2.4	Initialize POST Error Manager
C2	2.4	Initialize Error Logging
C3	2.4	Initialize Error Display Function
C4	2.4	Initialize System Error Handler
E0	2.4	Initialize the Chipset
E1	2.4	Initialize the Bridge
E2	2.2, 2.4	Initialize the Processor
E3	3.2	Initialiize System Timer
E4	6.1	Initialize System I/O
E5	2.6	Check Force Recovery Boot
E6	4.2	Checksum BIOS ROM
E7	4.0	Go To BIOS
E8	2.6	Set Huge Segment
E9	2.4, 2.7	Initialize Multiprocessor
EA	2.4, 2.7	Initialize OEM Special Code
EB	2.4	Initialize PIC & DMA
EC	5.1	Initialize Memory Type
ED	5.1	Initialize Memory Type
EE	5.1	Shadow Boot Block
EF	5.1	System Memory Test

HP Pavillion Series 3100 & 8000 PCs Continued		
F0	2.7	Initialize Interrupt Vectors
F1	2.5	Initialize Runtime Clock
F2	7.0	Initialize Video
F3	2.4	Initialize Beeper
F4	4.1	Initialize BOOT
F5	5.1	Clear Huge Segment
F6	4.1	Boot to Mini-DOS
F7	4.1	Boot to Full DOS

HP Vectra BIOS

Post Code	Diag. Sect.	Description
01	2.0	LED
02	2.2	Test CPU Test
03	4.0	Test BIOS ROM
04	3.2, 5.0	Test RAM Refresh Timer
05	3.0, 5.0	Test RAM Interrupt
06	5.5	Shadow BIOS ROM
07	2.6	Test CMOS RAM
08	2.2	Test Internal Cache Memory
09	7.0	Initialize Video Card
10	5.0	Test External Cache
11	5.5	Shadow Option ROMs
12	5.0	Test Memory Subsystem
13	2.1, 5.4	Initialize EISA/ISA Cards
14	8.1	Keyboard Controller Self-Test
15	3.2	Test Timer 0/Timer 2
16	5.7	Test DMA Subsystem
17	3.2	Test Interrupt Controller
18	5.0	Test RAM Address Lines

HP Vectra BIOS Continued		
19	5.0	Size Extended Memory
20	5.2	Real Mode RAM Test
21	5.5	Test Shadow RAM
22	5.2	Protected Mode RAM Test
23	2.5	Test RTC
24	8.0	Test Keyboard
25	6.6	Mouse Test
26	5.4	Hard Drive Test
27	6.6	Test LAN
28	6.5	Test Floppy Controller
29	2.3	Internal NPU Test
30	2.3	Weitek NPU Test
31	2.5	Clock Speed Switching Test
32	6.2	Test Serial Port
33	6.3	Test Parallel Port

HP Vectra ES

Post Code	Diag. Sect.	Description
000F	2.2	286 CPU Bad
0010	4.2	Bad Checksum on ROM 0
0011	4.2	Bad Checksum on ROM 1
011X	2.5	RTC Register X is Bad
0120	2.5	RTC Failed to Tick
0240	2.6	CMOS/RTC Lost Power
0241	2.6	Invalid Checksum, IBM CMOS Area
0280	2.7	Invalid Checksum, HP CMOS Area
02XY	2.7	Bad CMOS Register, At XY-40
0301	8.1	8042 Failed to Accept Reset Command

HP Vectra ES Continued		
0302	8.1	8042 Failed to Respond To Reset
0303	8.1	8042 Failed on Reset
0311	8.1	8042 Didn't Accept "Write Cmd Byte"
0312	8.1	8042 Didn't Accept Data
0321	8.1	8042 Failed to Accept Scancode, Port 68
0322	8.1	8042 Failed to Respond To Scancode
0323	8.1	8042 Responded Incorrectly To Scancode
0331	8.1	8042 Failed to Accept Command, Port 6A
0332	8.1	8042 Failed to Generate SVC on Port 67
0333	8.1	8042 Generated Incorrect HPINT, Port 65
0334	8.1	8042 Failed R/W Register on Port 69
0335	8.1	8042 Failed To Generate HPINT on IRQ 15
0336	8.1	8042 Failed To Generate HPINT on IRQ 12
0337	8.1	8042 Failed To Generate HPINT on IRQ 11
0338	8.1	8042 Failed To Generate HPINT on IRQ 10
0339	8.1	8042 Failed To Generate HPINT on IRQ 7
033A	8.1	8042 Failed To Generate HPINT on IRQ 5
033B	8.1	8042 Failed To Generate HPINT on IRQ 4
033C	8.1	8042 Failed To Generate HPINT on IRQ 3
0341	8.1	8042 Failed Keyboard Interface Test Cmd
0342	8.1	8042 Didn't respond to Interface Cmd
0343	8.1	Keyboard Clock Line Stuck Low
0344	8.1	Keyboard Clock Line Stuck High
0345	8.1	Keyboard Data Line Stuck Low
0346	8.1	Keyboard Data Line Stuck High
0350	8.1	No Ack from Keyboard Self-Test Cmd
0351	8.1	Bad Ack from Keyboard Self-Test Cmd
0352	8.1	Keyboard is Dead or Not Connected
0353	8.1	No Result from Keyboard Self-Test Cmd
0354	8.1	Keyboard Self-Test Failed

HP Vectra ES Continued		
0401	8.2	8042 Failed to Enable Gate A-20
0503	6.2	Serial Port Dead or Non-Existent
0505	6.2	Serial Port Fails Port Register Tests
0543	6.3	Parallel Port Dead or Non-Existent
06XX	8.1	Stuck Key. XX=Scancode Of Key
0700	3.2	Failed to Switch to Slow Mode
0701	3.2	Failed to Switch to Dynamic Mode
0702	3.2	Timer (Channel 0) Failed to Interrupt
0703	7.0	Mem Cycles too slow in Slow Mode
0704	7.0	Mem Cycles too fast In Slow Mode
0705	7.0	I/O Cycles too slow In Slow Mode
0706	7.0	I/O Cycles too fast In Slow Mode
0707	7.0	Mem Cycles too slow In Dynamic Mode
0708	7.0	Mem Cycles too fast In Dynamic Mode
0709	7.0	I/O Cycles too slow In Dynamic Mode
070A	7.0	I/O Cycles too fast In Dynamic Mode
110X	3.2	Timer X (0-2) Failed To Register Test
1200	5.1	Memory Refresh Signal Stuck High
1201	5.1	Memory Refresh Signal Stuck Low
211X	5.7	DMA 1 Failed R/W Test at Reg. X (0-7)
212X	5.7	DMA 2 Failed R/W Test at Reg. X (0-7)
221X	5.7	Bad DMA Page Register, X=Reg 0-7
300X	2.1	HP-HIL Controller Failed Self Test, X=Data
3010	5.4	HP-HIL Device Test Failed
4XYZ	5.1	Lower 640K Failed Read/Write Test For X=0,2,4,6 Y>0=Bad U23 Z>0=Bad U13 X=1,3,5,7 Y>0=Bad U43 Z>0=Bad U33 X=8 Y>0=Bad U22 Z>0=Bad U12 X=9 Y>0=Bad U42 Z>0=Bad U32
5XYZ	5.1	Lower 640K Failed Marching Ones Test. Same parameters as 4XYZ
61XY	5.1	RAM Address Line XY Stuck

HP Vectra ES Continued		
620X	5.1	Lower 640K Parity Error, Bank X
63XY	5.1	Parity Error Above 1MB, Bank XY
6400	5.1	Parity Generator Failed To Detect Error
71XY	3.1	Master 8259 Failed R/W, bits XY
72XY	3.1	Slave 8259 Failed R/W, Bits XY
7400	3.1	Master 8259 Failed Interrupt
7500	3.1	Slave 8259 Failed Interrupt

9XYZ	6.5	Floppy Controller Error, X=Drive #
		Y=0 = 1st Level Error
		Z=0= Unsuccessful Input from FD
		1= Unsuccessful output to FDC
		2= Error while executing seek
		3= Error during recalibrate
		4= Error verifying RAM buffer
		5= Error while resetting FDC
		6= Wrong drive identified
		7= Wrong media identified
		8= No interrupt from FDC
		9= Failed to detect Track 0
		A= Failed to detect index pulse
		Y>0 = Higher Level Error
		1, 2 = Read Sector Error, side 0 or 1
		3, 4 = Write Sector Error, side 0 or 1
		5, 6 = Format Sector Error, side 0 or 1
		7, 8 = Read ID Error, Side 0 or 1
		Z=1= No ID address mark
		2= No data address mark
		3= Media is write-protected
		4= Sector # wrong
		5= Cylinder # wrong
		6= Bad cylinder
		7= DMA over-run
		8= ID CRC error
		9= Data CRC error
		A= End of cylinder
		B= Unrecognizable error

A001	2.3	No 80287 Detected

HP Vectra ES Continued		
A002	2.3	80287 Failed Stack Register R/W Test
A00C	2.3	No Zero-Divide Interrupt from 80287
CXYZ	5.1	R/W Error on Extended RAM in XY Bank
CFFF	5.1	Ext. RAM Marching Ones Failure

HP Vectra QS & RS

Post Code	Diag. Sect.	Description
000F	2.2	386 CPU Bad
0010	4.2	Bad Checksum on ROM 0
0011	4.2	Bad Checksum on ROM 1
011X	2.5	RTC Register X is Bad
0120	2.5	RTC Failed to Tick
0240	2.6	CMOS/RTC Lost Power
0241	2.6	Invalid Checksum, IBM CMOS Area
0280	2.7	Invalid Checksum, HP CMOS Area
02XY	2.6	Bad CMOS Register, at XY-40
0301	8.1	8042 Failed to Accept Reset Command
0302	8.1	8042 Failed to Respond To Reset
0303	8.1	8042 Failed On Reset
0311	8.1	8042 Didn't Accept "Write Cmd Byte"
0312	8.1	8042 Didn't Accept Data
0321	8.1	8042 Failed to Accept Scancode, Port 68
0322	8.1	8042 Failed to Respond to Scancode
0323	8.1	8042 Responded Incorrectly to Scancode
0331	8.1	8042 Failed to Accept Command, Port 6A
0332	8.1	8042 Failed to Generate SVC on Port 67
0333	8.1	8042 Generated Incorrect HPINT, Port 65
0334	8.1	8042 Failed R/W Register on Port 69
0335	8.1	8042 Failed to Generate HPINT on IRQ 15

HP Vectra QS & RS Continued		
0336	8.1	8042 Failed to Generate HPINT on IRQ 12
0337	8.1	8042 Failed to Generate HPINT on IRQ 11
0338	8.1	8042 Failed to Generate HPINT on IRQ 10
0339	8.1	8042 Failed to Generate HPINT on IRQ 7
033A	8.1	8042 Failed to Generate HPINT on IRQ 5
033B	8.1	8042 Failed to Generate HPINT on IRQ 4
033C	8.1	8042 Failed to Generate HPINT on IRQ 3
0341	8.1	8042 Failed Keyboard Interface Test Cmd
0342	8.1	8042 Didn't respond to Interface Cmd
0343	8.1	Keyboard Clock Line Stuck Low
0344	8.1	Keyboard Clock Line Stuck High
0345	8.1	Keyboard Data Line Stuck Low
0346	8.1	Keyboard Data Line Stuck High
0350	8.1	No Ack from Keyboard Self-Test Cmd
0351	8.1	Bad Ack from Keyboard Self-Test Cmd
0352	8.1	Keyboard is Dead or Not Connected
0353	8.1	No Result from Keyboard Self-Test Cmd
0354	8.1	Keyboard Self-Test Failed
0401	8.2	8042 Failed to Enable Gate A-20
0503	6.2	Serial Port Dead or Non-Existent
0505	6.2	Serial Port Fails Port Register Tests
06XX	8.1	Stuck Key. XX=Scancode Of Key
0700	8.4	Failed to Switch to Slow Speed
0701	8.4	Failed to Switch to Fast Speed
0702	3.2	Timer Failed to Interrupt
0703	2.5	CPU Clock Too Slow In Slow Speed
0704	2.5	CPU Clock Too Fast In Slow Speed
0707	2.5	CPU Clock Too Slow In Fast Speed
0708	2.5	CPU Clock Too Fast In Fast Speed
0709	3.2	Failed To Switch Bus Clock To ATCLK

HP Vectra QS & RS Continued		
110X	3.2	Timer X (0-2) Failed To Register Test
1200	5.1	Memory Refresh Signal Stuck High
1201	51	Memory Refresh Signal Stuck Low
211X	5.7	DMA 1 Failed R/W Test at Reg. X (0-7)
212X	5.7	DMA 2 Failed R/W Test at Reg. X (0-7)
221X	5.7	Bad DMA Page Register, X=Reg 0-7
300X	2.1	HP-HIL Contrlr Failed Self Test, X=Data
3010	5.4	HP-HIL Device Test Failed
4XYZ	5.1	Lower 640K Failed Read/Write Test X=0,2,4,6 Y>0=Bad U23 Z>0=Bad U13 X=1,3,5,7 Y>0=Bad U43 Z>0=Bad U33 X=8 Y>0=Bad U22 Z>0=Bad U12 X=9 Y>0=Bad U42 Z>0=Bad U32
5XYZ	5.1	Lower 640K Failed Marching Ones Test
61XY	5.1	RAM Address Line XY Stuck
620X	5.1	Lower 640K Parity Error, Bank X
63XY	5.1	Parity Error Above 1MB, Bank XY
6500	5.5	Shadow RAM Bad At BIOS Segment
6510	5.5	Shadow RAM Bad At HP EGA Segment
71XY	3.1	Master 8259 Failed R/W, bits XY
72XY	3.1	Slave 8259 Faileed R/W, Bits XY
7400	3.1	Master 8259 Failed Interrupt
7500	3.1	Slave 8259 Failed Interrupt
9XYZ	6.5	Floppy Controller Error, X=Drive # Y=0 = 1st Level Error Z=0= Unsuccessful Input from FD 1= Unsuccessful output to FDC 2= Error while executing seek 3= Error during recalibrate 4= Error verifying RAM buffer 5= Error while resetting FDC 6= Wrong drive identified 7= Wrong media identified 8= No interrupt from FDC

		9= Failed to detect Track 0 A= Failed to detect index pulse Y>0 = Higher Level Error 1, 2 = Read Sector Error, side 0 or 1 3, 4 = Write Sector Error, side 0 or 1 5, 6 = Format Sector Error, side 0 or 1 7, 8 = Read ID Error, Side 0 or 1 Z=1= No ID address mark 2= No data address mark 3= Media is write-protected

		4= Sector # wrong
		5= Cylinder # wrong
		6= Bad cylinder
		7= DMA over-run
		8= ID CRC error
		9= Data CRC error
		A= End of cylinder
		B= Unrecognizable error

A001	2.3	No 80287 Detected
A002	2.3	80287 Failed Stack Register R/W Test
A00C	2.3	No Zero-Divide Interrupt From 80287
AF00	2.3	Coprocessor Didn't Enter Protected Mode
AF01	2.3	Coprocessor Not Present
AF02	2.3	Coprocessor Fails Register Test
AF05	2.3	Coprocessor Fails Addition Test
AF06	2.3	Coprocessor Fails Interrupt Test
AF0C	2.3	Coprocessor Fails Interrupt Test
CXYZ	5.1	R/W Error on Extended RAM in XY Bank
CFFF	5.1	No Extended RAM Found
EXYZ	5.1	Ext. RAM Marching Ones Failure At XYZ

IBM AT BIOS

Post Code	Diag. Sect.	Description
02	4.2	ROM Checksum

IBM AT BIOS Continued		
03	2.6	CMOS Byte 0F
04	3.2	PIT Channel 0
05	3.2	PIT Channel 1
06	5.7	8237 DMA 0
07	5.7	8237 DMA 1
08	5.7	DMA 0,1
09	5.1	Memory Refresh
0B	8.1	8042
1E	2.6	Set Memory from CMOS
1F	5.1	Address Lines 19-23
20	5.2	Protected Mode
21	5.2	Return from Protected
22	7.0	Enable Video Adapter
23	7.0	Check for CGA, EGA, VGA
24	7.0	Return from Video Test
25	3.1	PIC IRQs 0-13
26	3.1	Check From NMI
27	4.0	Test the POST Logic (106)
28	3.1	NMI Interrupts (Error 107)
29	3.2	Test Timer 2 (Error 108)
2A	3.2	Do Test (Error 102)
2B	3.2	Too Fast (Error 102)
2C	3.2	Too Slow (Error 103)
2D	8.1	Test 8042 (Error 105)
2F	8.1	Test Reset Status
30	4.0	Set Shutdown Return 2
31	5.2	Enable Protected Mode
32	5.1	Address Lines 0-15
33	5.1	Next Block Of 64K
34	2.6	Restore Checkpoint

IBM AT BIOS Continued		
35	8.1	Keyboard Test
36	8.1	Check for AA Scan Code
38	8.1	Stuck Key Test
3A	8.1	Initialize 8042
3B	5.4	Check for ROM in 2K Blocks
3C	6.5	Check IPL Diskette Drive
3D	6.5	Initialize Floppy Drive
3E	6.4	Initialize Hard Drive
3F	6.3	Initialize Printer
40	3.2	Enable Interrupt for 80287
41	2.1, 4.0	Code Segment Code E000:0?
42	4.1	Exit to System Code
43	4.1	Go to Boot Loader
44	4.1	Boot from Fixed Disk
45	4.1	Unable to Boot, go to Basic
81	8.1	Build Descriptor Table
82	5.2	Switch to Virtual Mode
90-B6	4.1	Mem & Bootstrap Test
F0	2.6	Set Data Segment
F1	3.1, 3.2	Test Interrupt 32
F2	3.1, 3.2	Exception Interrupt 13D
F3	2.2	Verify 286 LDT/SDT, LTR/STR
F4	2.2	Verify 286 Bound Instruction
F5	2.2	Verify Push & Pop
F6	2.2	Verify Access Rights
F7	2.2	Verify APRL Functions
F8	2.2	Verify LAR Instruction
F9	2.2	Verify LSL Instruction
FA	5.1	Low Meg Chip Select Test

IBM PS/2 (MCA)

Post Code	Diag. Sect.	Description
00	2.2	CPU FFAA0055 Pattern Test
01	2.2	CPU Register Test
02	4.2	BIOS ROM Checksum
03	3.1	System Port 94 Enable/Check
04	2.1	POST Registers, Port 102 Enable/Check
05	2.1	POST Port 96 Enable/Check
06	2.6	Byte 0F CMOS (NMI Disable)
07	2.7	CMOS Extended Ports 74-76 Test
08	5.7	DMA Test (Ports 2,18,1A,1C)
09	5.7	Initialize DMA Chips
0A	5.1	Refresh Test (Port 61)
0B	8.1	8042 Buffer Test (Port 61,64)
0C	8.1	8042 Internal Test (Port 60)
0D	8.1	8042 Internal Test
0E	8.1	8042 Error Indicated (Port 64)
0F	5.1	Size Memory
10	5.1	Base Memory Test
11	5.1	Base Memory Error
12	8.1	Verify Keyboard Commands
13	3.1	Initialize PIC Master
14	3.1	Initialize PIC Slave
15	3.1, 4.0	Setup Vector Table
16	3.1, 4.0	Setup Extended Vector Table
17	2.6	CMOS Byte 0D Test
18	2.6	CMOS Checksum Test
19	2.6	CMOS Byte 0D<80H
1A	8.1	Check Soft/Hard Reset
1B	5.2	Protected Mode Initialization

IBM PS/2 (MCA) Continued		
1C	5.2	Set Stack For Protected Mode
1D	5.1	Size Base Memory
1E	2.6	Save Memory Size
1F	2.6, 5.1	Setup Memory Split Address
20	5.1	Determine Memory Above 64MG
21	5.1	Memory Address Line Test
22	3.1	Disable NMI
23	3.2	Initialize System Timer
24	2.6	Determine CMOS Validity
25	8.1	Write 8042 Command Byte
40	2.6, 7.3	Check CMOS And Video
41	1.0, 2.6	Display Error 160
42	3.1	PIC Master/Slave Test
43	3.1	PIC Master/Slave Test
44	3.1	Check for NMI when Disabled
45	3.1	Test NMI
46	3.1	NMI Error Detected
47	3.2	System Timer Test
48	5.1	Speaker Bit Stuck Test
49	3.2	Timer 0 Test
4A	3.2	Timer 2 Test
4B	3.2	Timer Interrupt Occurred
4C	3.2	Timer 0 Fast/Slow Test
4D	3.2	Timer 0 Interrupt Test
4E	8.1	8042 Buffer Free
4F	8.1	8042 Soft/Hard Reset
50	5.2	Prepare For Protected Mode
51	5.2	Enter Protected Mode
52	5.2	Protected Memory Test
53	5.1	Memory Test Complete

IBM PS/2 (MCA) Continued		
54	5.2	Exit Protected Mode
55	2.0	Test for Loop
56	8.1	8042 Disable
57	8.1	8042 Self Test Command
58	8.1	8042 Check For Errors
59	8.1	Keyboard Test
5A	6.2	Initialize Mouse
5B	6.2	Disable Mouse
5C	3.1, 4.0	Initialize BIOS Vectors
5D	3.1, 4.0	Initialize BIOS Vectors
5E	3.1, 4.0	Initialize BIOS Vectors
5F	5.5	BIOS Data Area
60	6.5	Determine Diskette Rate
61	6.5	Reset Floppy Controller
62	6.5	Floppy Drive Test
63	6.5	Floppy Motor Disable
64	6.2	RS232 Setup
65	2.6	RTC Interrupt Test
66	6.5	Floppy Drive Setup
67	6.4	Hard Drive Setup
68	2.4	Initialize CPU Wait States
69	5.4	Determine Optional ROMS
6A	6.2	Determine RS232/Parallel Ports
6B	2.6	Set Up Equipment List
6C	2.6, 5.4	Configuration Error Reported
6D	8.1	Set Typematic Rate
6E	4.1	INT 19 Boot loader
70	6.4	Reset Disk
71	4.1	Read Boot code for E6/E9
72	4.1	Control To Boot code

IBM PS/2 (MCA) Continued		
73	4.1	Boot code/ROM Basic

Intel CA810E BIOS

Uncompressed INIT Code Checkpoints

Post Code	Description
D0	NMI is disabled. Onboard keyboard controller and real time clock enabled (if present). Initialization code checksum verification starting
D1	Keyboard controller BAT test, CPU ID saved, and going to 4GB flat mode
D3	Initialize chipset, start memory refresh, and determine memory size
D4	Verify base memory
D5	Initialization code to be copied to segment 0 and control to be transferred to segment 0
D6	Control is in segment 0. Used to check if in recovery mode and to verify main BIOS checksum. If in recovery mode or if main BIOS checksum is wrong, go to checkpoint E0 for recovery. Otherwise, got o checkpoint D7 to give control to main BIOS
D7	Find main BIOS module in ROM image
D8	Uncompress the main BIOS module
D9	Copy main BIOS image to F000 shadow RAM and give control to main BIOS in F000 shadow RAM

Intel CA810E Boot Block Recovery Code

Post Code	Description
E0	Onboard disk controller (if any) is initialized. Compressed recovery code is uncompressed at F000:0000 in shadow RAM. Give control to recovery code at F000 in shadow RAM. Initialize interrupt vector tables, system timer, DMA controller, and interrupt controller

Intel CA810E Runtime Code Continued	
E8	Initialize extra (Intel recovery) module
E9	Initialize diskette drive
EA	Try to boot from diskette. If reading of boot sector is successful, give control to boot sector code
EB	Boot from diskette failed; look for ATAPI (LS-120, Zip) devices
EC	Try to boot from ATAPI device. If reading of boot sector is successful, give control to boot sector code
EF	Boot from diskette and ATAPI device failed. Give two beeps. Retry the booting procedure (go to checkpoint E9)

Intel CA810E Runtime Code

Uncompressed in F000 Shadow RAM

Post Code	Description
03	NMI is disabled. To check soft reset/power on
05	BIOS stack set. Going to disable cache if any
06	POST code to be uncompressed
07	CPU init and CPU data area init to be done
08	CMOS checksum calculation to be done next
0B	Any initialization before keyboard BAT to be done next
0C	Keyboard controller I/B free. To issue the BAT command to the keyboard controller
0E	Any initialization after keyboard controller BAT to be done next
0F	Keyboard command byte written
10	Going to issue Pin 23, 24 blocking/unblocking command
11	Going to check pressing of <INS>, <END> key during power-on
12	To init CMOS if "Init CMOS in every boot" is set or <END> key is pressed. Going to disable DMA and interrupt controllers

Intel CA810E Runtime Code Continued	
13	Video display is disabled and port B is initialized. Chipset init about to begin
14	8254 timer test about to start
19	About to start memory refresh test
1A	Memory refresh line is toggling. Going to check 15 µs On/OFF time
23	To read 8042 input port and disable mega key Green PC feature. Make BIOS cade segment writeable
24	To do any setup before int vector init
25	Interrupt vector initialization to begin. To clear password if necessary
27	Any initialization before set video mode to be done
28	Going for monochrome mode and color mode setting
2A	Different buses init (system, static, output devices) to start if present
2B	To give control for any setup required before optional ROM check
2C	To look for optional video ROM and give control
2D	To give control to do any processing after video ROM returns control
2E	If EGA/VGA not found then do display memory R/W
2F	EGA/VGA not found. Display memory R/W test about to begin
30	Display memory R/W test passed. About to look for the retrace checking
31	Display memory R/W test or retrace checking failed. To do alternate Display memory R/W test
32	Alternate Display memory R/W test passed. To look for the alternate display retrace checking
34	Video display check over. Display mode to be set next
37	Display mode set. Going to display power on message
38	Different buses init (input, IPL, general devices) to start if present

Intel CA810E Runtime Code Continued	
39	Display different buses initialization error messages
3A	New cursor position read and saved. To display the Hit <DEL> message
40	To prepare the descriptor tables
42	To enter virtual mode for memory test
43	To enable interrupts for diagnostics mode
44	To initialize data to check memory wrap around at 0:0
45	Data initialized. Going to check for memory wrap around at 0:0 and finding the total system test memory
46	Memory wrap around test done. Memory size calculation over. About to go for writing patterns to test memory.
47	Pattern to be tested written in extended memory. Going to write patterns in base 640KB memory
48	Patterns written in base memory. Going to find out amount of memory below 1M memory
49	Amount of memory below 1M found and verified. Going to find out amount of memory above 1M
4B	Amount of memory above 1M found and verified. Check for soft reset and going to clear memory below 1M for soft reset. (If power on, go to check point # 4E
4C	Memory below 1M cleared. (SOFT RESET) Going to clear memory above 1M
4D	Memory above 1M cleared (SOFT RESET) Going to save the memory size (Go to check point # 52
4E	Memory test started. (NOT SOFT RESET) About to display the first 64KB memory size
4F	Memory size display started. This will be updated during memory test. Going for sequential & random memory test
50	Memory testing/initialization below 1MB complete. Adjust displayed memory size for relocation shadow
51	Memory size display adjusted due to relocation/shadow. Memory test above 1MB to follow
52	Memory testing/initialization above 1MB complete. Going to save memory size information

Intel CA810E Runtime Code Continued	
53	Memory size information is saved. CPU registers are saved. Going to enter real mode
54	Shutdown successful, CPU in real mode. Going to disable gate A20 line and disable parity/NMI
57	A20 address line, parity/NMI disable successful. Going to adjust memory size depending on relocation/shadow
58	Memory size adjusted for relocation/shadow. Going to clear hit <DEL> message
59	Hit <DEL> message cleared. <WAIT...> message displayed. About to start DMA and interrupt controller test
60	DMA page register test passed. To do DMA #1 base register test
62	DMA #1 base register test passed. To do DMA #2 base register test
65	DMA #2 base register test passed. To program DMA #1 and #2
66	DMA #1 and #2 programming over. To initialize 8259 interrupt controller
7F	Extended NMI sources enabling is in progress
80	Keyboard test started. Clearing output buffer, checking for stuck key, to issue keyboard reset command
81	Keyboard reset error/stuck key found. To issue keyboard controller interface test command
82	Keyboard controller interface test over. To write command byte and init circular buffer
83	Command byte written, global data init done. To check for lock-key
84	Lock key checking over. to check for memory size mismatch with CMOS
85	Memory size check done. to display soft error and check for password or bypass setup
86	Password checked. About to do programming before setup
87	Programming before setup complete. To uncompress SETUP code and execute CMOS setup

Intel CA810E Runtime Code Continued	
88	Returned from CMOS setup program and screen is cleared. About to do programming after setup
89	Programming after setup complete. Going to display power-on screen message
8B	First screen message displayed. <WAIT...> message displayed. PS/2 mouse check and extended BIOS data area allocation to be done
8C	Setup options programming after CMOS setup about to start
8D	Going to hard disk controller reset
8F	Hard disk controller reset done. Floppy setup done next
91	Floppy setup complete. Hard disk setup next
95	Init of different buses optional ROMs from C800 to start.
96	Going to do any init before C800 optional ROM control
97	Any init before C800 optional ROM control is over. Optional ROM check and control will be done next
98	Optional ROM control is done. About to give control to do any required processing after optional ROM returns control and enable external cache
99	Any initialization required after optional ROM test over. Going to setup timer data area and printer base address
9A	Return after setting timer and printer base addresses. Going to set the RS-232 base address
9B	Returned after RS-232 base address. Going to do any initialization before coprocessor test
9C	Required initialization before coprocessor is over. Going to initialize the coprocessor test
9D	Coprocessor initialized. Going to do any initialization after coprocessor test
9E	Initialization after coprocessor test is complete. Going to check extended keyboard, keyboard ID and num-lock
A2	Going to display any soft errors
A3	Soft error display complete. Going to set keyboard typematic rate

Intel CA810E Runtime Code Continued	
A4	Keyboard typematic rate set. To program memory wait states
A5	Going to enable parity/NMI
A7	NMI and parity enabled. Going to do any initialization required before giving control to optional ROM at E000
A8	Initialization before E000 ROM control over. E000 ROM to get control next
A9	Returned from E000 ROM control. Going to do any initialization required after E000 optional ROM control
AA	Initialization after E000 optional ROM control is over. Going to display the system configuration
AB	Put Int13 module runtime image to shadow
AC	Generate MP for multiprocessor support (if present)
AD	Put CGA Int10 module (if present) in shadow
AE	Uncompress SMBIOS module and init SMBIOS code and form the runtime SMBIOS image in shadow
B1	Going to copy any code to specific area
00	Copying of code to specific area done. Going to give control to Int19 boot loader

Intel CC820 BIOS

Uncompressed INIT Code Checkpoints

Post Code	Description
D0	NMI is disabled. Onboard KBC, RTC enabled (if present). Init code checksum verification starting
D1	Keyboard controller BAT test, CPU ID saved, and going to 4GB flat mode
D3	Do necessary chipset initialization, start memory refresh, and do memory sizing
D4	Verify base memory
D5	Init code to be copied to segment 0 and control to be transferred to segment 0

Intel CC820 BIOS Continued	
D6	Control is in segment 0. To check recovery mode and verify main BIOS checksum. If either it is recovery mode or main BIOS checksum is bad, go to check point E0 for recovery else go to check point D7 for giving control to main BIOS.
D7	Find main BIOS module in ROM image
D8	Uncompress the main BIOS module
D9	Copy main BIOS image to F000 shadow RAM and give control to admin BIOS in F000 shadow RAM

Intel CC820 Boot Block Recovery

Post Code	Description
E0	Onboard floppy controller (if any) is initialized. Compressed recovery code is uncompressed in F000:0000 in shadow RAM and give control to recovery code in F000 shadow RAM. Initialize interrupt vector tables, initialize system timer, initialize DMA controller and interrupt controller
E8	Initialize extra (Intel Recovery) Module
E9	Initialize floppy drive
EA	Try to boot from floppy
EB	Booting from floppy failed, look for ATAPI (LS120, Zip) devices
EC	Try to boot from ATAPI. If reading boot sector is successful, give control to boot sector code
EF	Booting from floppy failed and ATAPI device failed. Give two beeps. Retry the booting procedure again (go back to check point E9)

Intel CC820 Runtime Code

Uncompressed in F000 Shadow RAM

Post Code	Description
03	NMI is disabled. To check soft reset/power on
05	BIOS stack set. Going to disable cache if any
06	POST code to be uncompressed
07	CPU init and CPU data area init to be done
08	CMOS checksum calculation to be done next
0B	Any initialization before keyboard BAT to be done next
0C	Keyboard controller I/B free. To issure the BAT command to the keyboard controller
0E	Any initialization after keyboard controller BAT to be done next
0F	Keyboard command byte written
10	Going to issue Pin 23, 24 blocking/unblocking command
11	Going to check pressing of <INS>, <END> key during power-on
12	To init CMOS if "Init CMOS in every boot" is set or <END> key is pressed. Going to disable DMA and interrupt controllers
13	Video display is disabled and port B is initialized. Chipset init about to begin
14	8254 timer test about to start
19	About to start memory refresh test
1A	Memory refresh line is toggling. Going to check 15 µs On/OFF time
23	To read 8042 input port and disable mega key Green PC feature. Make BIOS cade segment writeable
24	To do any setup before int vector init
25	Interrupt vector initialization to begin. To clear password if necessary
27	Any initialization before setting video mode to be done

Intel CC820 Runtime Code Continued	
28	Going for monochrome mode and color mode setting
2A	Different buses init (system, static, output devices) to start if present
2B	To give control for any setup required before optional ROM check
2C	To look for optional video ROM and give control
2D	To give control to do any processing after video ROM returns control
2E	If EGA/VGA not found then do display memory R/W
2F	EGA/VGA not found. Display memory R/W test about to begin
30	Display memory R/W test passed. About to look for the retrace checking
31	Display memory R/W test or retrace checking failed. To do alternate Display memory R/W test
32	Alternate Display memory R/W test passed. To look for the alternate display retrace checking
34	Video display checking over. Display mode set next
37	Display mode set. Going to display power on message
38	Different buses init (input, IPL, general devices) to start if present
39	Display different buses initialization error messages
3A	New cursor position read and saved. To display the Hit <DEL> message
40	To prepare the descriptor tables
42	To enter virtual mode for memory test
43	To enable interrupts for diagnostics mode
44	To initialize data to check memory wrap around at 0:0
45	Data initialized. Going to check for memory wrap around at 0:0 and finding the total system test memory
46	Memory wrap around test done. Memory size calculation over. About to go for writing patterns to test memory.

Intel CC820 Runtime Code Continued	
47	Pattern to be tested written in extended memory. Going to write patterns in base 640KB memory
48	Patterns written in base memory. Going to find out amount of memory below 1M memory
49	Amount of memory below 1M found and verified. Going to find out amount of memory above 1M
4B	Amount of memory above 1M found and verified. Check for soft reset and going to clear memory below 1M for soft reset. (If power on, go to check point # 4E
4C	Memory below 1M cleared. (SOFT RESET) Going to clear memory above 1M
4D	Memory above 1M cleared (SOFT RESET) Going to save the memory size (Go to check point # 52)
4E	Memory test started. (NOT SOFT RESET) About to display the first 64KB memory size
4F	Memory size display started. This is updated during memory test. Sequential and random memory test
50	Memory testing/initialization below 1MB complete. Going to adjust displayed memory size for relocation shadow
51	Memory size display adjusted due to relocation/shadow. Memory test above 1MB to follow
52	Memory testing/initialization above 1MB complete. Going to save memory size information
53	Memory size information is saved. CPU registers are saved. Going to enter real mode
54	Shutdown successful, CPU in real mode. Going to disable gate A20 line and disable parity/NMI
57	A20 address line, parity/NMI disable successful. Going to adjust memory size depending on relocation/shadow
58	Memory size adjusted for relocation/shadow. Going to clear hit <DEL> message
59	Hit <DEL> message cleared. <WAIT...> message displayed. About to start DMA and interrupt controller test
60	DMA page reg test passed. To do DMA #1 base reg test

Intel CC820 Runtime Code Continued	
62	DMA #1 base register test passed. To do DMA #2 base register test
65	DMA #2 base register test passed. To program DMA #1 and #2
66	DMA #1 and #2 programming over. To initialize 8259 interrupt controller
7F	Extended NMI sources enabling is in progress
80	Keyboard test started. Clearing output buffer, checking for stuck key, to issue keyboard reset command
81	Keyboard reset error/stuck key found. To issue keyboard controller interface test command
82	Keyboard controller interface test over. To write command byte and init circular buffer
83	Command byte written, global data init done. To check for lock-key
84	Lock key checking over. To check for memory size mismatch with CMOS
85	Memory size check done. To display soft error and check for password or bypass setup
86	Password checked. About to do programming before setup
87	Programming before setup complete. To uncompress SETUP code and execute CMOS setup
88	Returned from CMOS setup program and screen is cleared. About to do programming after setup
89	Programming after setup complete. Going to display power-on screen message
8B	First screen message displayed. <WAIT...> message displayed. PS/2 mouse check and extended BIOS data area allocation to be done
8C	Setup options programming after CMOS setup about to start
8D	Going to hard disk controller reset
8F	Hard disk controller reset done. Floppy setup to be done next

Intel CC820 Runtime Code Continued	
91	Floppy setup complete. Hard disk setup done next
95	Init of different buses optional ROMs from C800 to start.
96	Going to do any init before C800 optional ROM control
97	Any init before C800 optional ROM control is over. Optional ROM check and control will be done next
98	Optional ROM control is done. About to give control to do any required processing after optional ROM returns control and enable external cache
99	Any initialization required after optional ROM test over. Going to setup timer data area and printer base address
9A	Return after setting timer and printer base addresses. Going to set the RS-232 base address
9B	Returned after RS-232 base address. Going to do any initialization before coprocessor test
9C	Required initialization before coprocessor is over. Going to initialize the coprocessor test
9D	Coprocessor initialized. Going to do any initialization after coprocessor test
9E	Initialization after coprocessor test is complete. Going to check extended keyboard, keyboard ID and num-lock
A2	Going to display any soft errors
A3	Soft error display complete. Going to set keyboard typematic rate
A4	Keyboard typematic rate set. To program memory wait states
A5	Going to enable parity/NMI
A7	NMI and parity enabled. Going to do any initialization required before giving control to optional ROM at E000
A8	Initialization before E000 ROM control over. E000 ROM to get control next
A9	Returned from E000 ROM control. Going to do any initialization required after E000 optional ROM control
AA	Initialization after E000 optional ROM control is over. Going to display the system configuration

Intel CC820 Runtime Code Continued	
AB	Put Int13 module runtime image to shadow
AC	Generate MP for multiprocessor support (if present)
AD	Put CGA Int10 module (if present) in shadow
AE	Uncompress SMBIOS module and init SMBIOS code and form the runtime SMBIOS image in shadow
B1	Going to copy any code to specific area
00	Copying of code to specific area done. Going to give control to Int19 boot loader

Intel SE440BX-2 BIOS

Uncompressed INIT Code Checkpoints

Post Code	Description
02	Verify real mode
03	Disable non maskable interrupts (NMIs)
04	Get processor type
06	Initialize system hardware
08	Initialize chipset with initial POST values
09	Set IN POST flag
0A	Initialize CPU registers
0B	Enable CPU cache
0C	Initialize caches to initial POST values
0E	Initialize I/O component
0F	Initialize the local bus IDE
10	Initialize Power Management
11	Load alternate registers with initial POST values new
12	Restore CPU control word during warm boot
13	Initialize PCI bus mastering devices
14	Initialize keyboard controller
16	BIOS ROM checksum
17	Initialize cache before memory auto size

Intel SE440BX-2 BIOS Continued	
18	8254 timer initialization
1A	8237 DMA controller initialization
1C	Reset programmable interrupt controller
20	Test DRAM refresh
22	Test keyboard controller
24	Set ES segment register to 4GB
26	Enable A20 line
28	Auto size DRAM
29	Initialize POST memory manager
2A	Clear 512KB base RAM
2C	RAM failure on address line xxxx
2E	RAM failure on data bits xxxx of low byte of memory bus
2F	Enable cache before system BIOS shadow
30	RAM failure on data bits xxxx of high byte of memory bus
32	Test CPU bus-clock frequency
33	Initialize POST dispatch manager
34	Test CMOS RAM
35	Initialize alternate chipset registers
36	Warm start shut down
37	Reinitialize the chipset (motherboard only)
38	Shadow system BIOS ROM
39	Reinitialize the cache (motherboard only)
3A	Auto size cache
3C	Configure advanced chipset registers
3D	Load alternate registers with CMOS values new
40	Set initial CPU speed new
42	Initialize interrupt vectors
44	Initialize BIOS interrupts
45	POST device initialization
46	Check ROM copyright notice

Intel SE440BX-2 BIOS Continued	
47	Initialize manager for PCI option ROMs
48	Check video configuration against CMOS RAM data
49	Initialize PCI bus and devices
4A	Initialize all video adapters in system
4B	Display Quiet Boot screen
4C	Shadow video BIOS ROM
4E	Display BIOS copyright notice
50	Display CPU type and speed
51	Initialize EISA motherboard
52	Test keyboard
54	Set key click if enabled
56	Enable keyboard
58	Test for unexpected interrupts
59	Initialize POST display service
5A	Display prompt "Press F2 to enter SETUP"
5B	Disable CPU cache
5C	Test RAM between 512 KB and 640 KB
60	Test extended memory
62	Test extended memory address lines
64	Jump to User Patch 1
66	Configure advanced cache registers
67	Initialize multiprocessor APIC
68	Enable external and processor caches
69	Setup System Management Mode (SMM)
6A	Display external L2 cache size
6C	Display shadow area message
6E	Display possible high address for UMB recovery
70	Display error messages
72	Check for configuration errors
74	Test real time clock

Intel SE440BX-2 BIOS Continued	
76	Check for keyboard errors
7A	Test for key lock on
7C	Setup hardware interrupt vectors
7E	Initialize coprocessor if present
80	Disable onboard Super I/O ports and IRQs
81	Late POST device initialization
82	Detect and install external RS232 ports
83	Configure non-MCD IDE controllers
84	Detect and install external parallel ports
85	Initialize PC compatible PnP ISA devices
86	Reinitialize onboard I/O ports
87	Configure motherboard configurable devices
88	Initialize BIOS Data Area
89	Enable non maskable interrupts
8A	Initialize extended BIOS Data Area
8B	Test and initialize PS/2 mouse
8C	Initialize floppy controller
8F	Determine number of ATA drives
90	Initialize hard disk controllers
91	Initialize local bus hard disk controllers
92	Jump to User Patch 2
93	Build MPTABLE for multiprocessor boards
94	Disable A20 address line
95	Install CD-ROM for boot
96	Clear huge ES segment register
97	Fix up multiprocessor table
98	Search for option ROMs
99	Check for SMART drives
9A	Shadow option ROMs
9C	Setup power management

Intel SE440BX-2 BIOS Continued	
9E	Enable hardware interrupts
9F	Determine number of ATA and SCSI drives
A0	Set time of day
A2	Check key lock
A4	Initialize typmatic rate
A8	Erase F2 prompt
AA	Scan for F2 keystroke
AC	Enter SETUP
AE	Clear IN POST flag
B0	Check for errors
B2	POST done - prepare to boot operating system
B4	One short beep before boot
B5	Terminate Quiet Boot
B6	Check password (optional)
B8	Clear global descriptor table
B9	Clean up all graphics
BA	Initialize DMI parameters
BB	Initialize PnP option ROMs
BC	Clear parity checkers
BD	Display Multi Boot menu
BE	Clear screen (optional)
BF	Check virus and backup reminders
C0	Try to boot with INT 19h
C1	Initialize POST Error Manager (PEM)
C2	Initialize error logging
C3	Initialize error display function
C4	Initialize system error handler
E0	Initialize the chipset
E1	Initialize the bridge
E2	Initialize the processor

Intel SE440BX-2 BIOS Continued	
E3	Initialize the system timer
E4	Initialize system I/O
E5	Check force recovery boot
E6	Checksum BIOS ROM
E7	Go to BIOS
E8	Set huge segment
E9	Initialize multiprocessor
EA	Initialize OEM special code
EB	Initialize PIC and DMA
EC	Initialize memory type
ED	Initialize memory size
EE	Shadow boot block
EF	System memory size
F0	Initialize interrupt vectors
F1	Initialize runtime clock
F2	Initialize video
F3	Initialize beeper
F4	Initialize boot
F5	Clear huge segment
F6	Boot to mini-DOS
F7	Boot to full DOS

Intel D810E2CB BIOS

Uncompressed INIT Code Checkpoints

Post Code	Description
D0	NMI is disabled. Onboard keyboard controller and real time clock enabled (if present). Initialization code checksum verification starting
D1	Keyboard controller BAT test, CPU ID saved, and going to 4GB flat mode

Intel D810E2CB BIOS Continued	
D3	Initialize chipset, start memory refresh, and determine memory size
D4	Verify base memory
D5	Initialization code to be copied to segment 0 and control to be transferred to segment 0
D6	Control is in segment 0. Used to check if in recovery mode and to verify main BIOS checksum. If in recovery mode or if main BIOS checksum is wrong, go to checkpoint E0 for recovery. Otherwise, got o checkpoint D7 to give control to main BIOS
D7	Find main BIOS module in ROM image
D8	Uncompress the main BIOS module
D9	Copy main BIOS image to F000 shadow RAM and give control to main BIOS in F000 shadow RAM

Intel D810E2CB Boot Block Recovery

Post Code	Description
E0	Onboard diskette controller (if any) is initialized. Compressed recovery code is uncompressed at F000:0000 in shadow RAM. Give control to recovery code at F000 in shadow RAM. Initialize interrupt vector tables, system timer, DMA controller, and interrupt controller
E8	Initialize extra (Intel recovery) module
E9	Initialize diskette drive
EA	Try to boot from diskette. If reading of boot sector is successful, give control to boot sector code
EB	Boot from diskette failed; look for ATAPI (LS-120, Zip) devices
EC	Try to boot from ATAPI device. If reading of boot sector is successful, give control to boot sector code
EF	Boot from diskette and ATAPI device failed. Give two beeps. Retry the booting procedure (go to checkpoint E9)

Intel D810E2CB Runtime Code

Uncompressed in F000 Shadow RAM

Post Code	Description
03	NMI is disabled. To check soft reset/power on
05	BIOS stack set. Going to disable cache if any
06	POST code to be uncompressed
07	CPU init and CPU data area init to be done
08	CMOS checksum calculation to be done next
0B	Any initialization before keyboard BAT done next
0C	Keyboard controller I/B free. To issure the BAT command to the keyboard controller
0E	Any initialization after keyboard controller BAT to be done next
0F	Keyboard command byte written
10	Going to issue Pin 23, 24 blocking/unblocking command
11	Going to check pressing of <INS>, <END> key during power-on
12	To init CMOS if "Init CMOS in every boot" is set or <END> key is pressed. Going to disable DMA and interrupt controllers
13	Video display is disabled and port B is initialized. Chipset init about to begin
14	8254 timer test about to start
19	About to start memory refresh test
1A	Memory refresh line is toggling. Going to check 15 µs On/OFF time
23	To read 8042 input port and disable mega key Green PC feature. Make BIOS cade segment writeable
24	To do any setup before int vector init
25	Interrupt vector initialization to begin. To clear password if necessary
27	Any initialization before setting video mode to be done

Intel D810E2CB Runtime Continued	
28	Going for monochrome mode and color mode setting
2A	Different buses init (system, static, output devices) to start if present
2B	To give control for any setup required before optional ROM check
2C	To look for optional video ROM and give control
2D	To give control to do any processing after video ROM returns control
2E	If EGA/VGA is not found then do display memory R/W
2F	EGA/VGA not found. Display memory R/W test about to begin
30	Display memory R/W test passed. About to look for the retrace checking
31	Display memory R/W test or retrace checking failed. To do alternate Display memory R/W test
32	Alternate Display memory R/W test passed. To look for the alternate display retrace checking
34	Video display checking over. Display mode to be set next
37	Display mode set. Going to display the power on message
38	Different buses init (input, IPL, general devices) to start if present
39	Display different BUS' initialization error messages
3A	New cursor position read and saved. To display the Hit <DEL> message
40	To prepare the descriptor tables
42	To enter virtual mode for memory test
43	To enable interrupts for diagnostics mode
44	To initialize data to check memory wrap around at 0:0
45	Data initialized. Going to check for memory wrap around at 0:0 and finding the total system test memory
46	Memory wrap around test done. Memory size calculation over. About to go for writing patterns to test memory.

Intel D810E2CB Runtime Continued	
47	Pattern to be tested written in extended memory. Going to write patterns in base 640KB memory
48	Patterns written in base memory. Going to find out amount of memory below 1M memory
49	Amount of memory below 1M found and verified. Going to find out amount of memory above 1M memory
4B	Amount of memory above 1M found and verified. Check for soft reset and going to clear memory below 1M for soft reset. (If power on, go to check point # 4E
4C	Memory below 1M cleared. (SOFT RESET) Going to clear memory above 1M
4D	Memory above 1M cleared (SOFT RESET) Going to save the memory size (Go to check point # 52
4E	Memory test started. (NOT SOFT RESET) About to display the first 64KB memory size
4F	Memory size display started. This will be updated during memory test. Going for sequential and random memory test
50	Memory testing/initialization below 1MB complete. Going to adjust displayed memory size for relocation shadow
51	Memory size display adjusted due to relocation/shadow. Memory test above 1MB to follow
52	Memory testing/initialization above 1MB complete. Going to save memory size information
53	Memory size information is saved. CPU registers are saved. Going to enter real mode
54	Shutdown successful, CPU in real mode. Going to disable gate A20 line and disable parity/NMI
57	A20 address line, parity/NMI disable successful. Going to adjust memory size depending on relocation/shadow
58	Memory size adjusted for relocation/shadow. Going to clear hit <DEL> message
59	Hit <DEL> message cleared. <WAIT...> message displayed. About to start DMA and interrupt controller test

Intel D810E2CB Runtime Continued	
60	DMA page register test passed. To do DMA #1 base register test
62	DMA #1 base register test passed. To do DMA #2 base register test
65	DMA #2 base register test passed. To program DMA #1 and #2
66	DMA #1 and #2 programming over. To initialize 8259 interrupt controller
7F	Extended NMI sources enabling is in progress
80	Keyboard test started. Clearing output buffer, checking for stuck key, to issue keyboard reset command
81	Keyboard reset error/stuck key found. To issue keyboard controller interface test command
82	Keyboard controller interface test over. To write command byte and init circular buffer
83	Command byte written, global data init done. To check for lock-key
84	Lock key checking over. To check for memory size mismatch with CMOS
85	Memory size check done. To display soft error and check for password or bypass setup
86	Password checked. About to do programming before setup
87	Programming before setup complete. To uncompress SETUP code and execute CMOS setup
88	Returned from CMOS setup program and screen is cleared. About to do programming after setup
89	Programming after setup complete. Going to display power-on screen message
8B	First screen message displayed. <WAIT...> message displayed. PS/2 mouse check and extended BIOS data area allocation to be done
8C	Setup options programming after CMOS setup about to start
8D	Going to hard disk controller reset

Intel D810E2CB Runtime Continued	
8F	Hard disk controller reset done. Floppy setup to be done next
91	Floppy setup complete. Hard disk setup done next
95	Init of different buses optional ROMs from C800 to start.
96	Going to do any init before C800 optional ROM control
97	Any init before C800 optional ROM control is over. Optional ROM check and control will be done next
98	Optional ROM control is done. About to give control to do any required processing after optional ROM returns control and enable external cache
99	Any initialization required after optional ROM test over. Going to setup timer data area and printer base address
9A	Return after setting timer and printer base addresses. Going to set the RS-232 base address
9B	Returned after RS-232 base address. Going to do any initialization before coprocessor test
9C	Required initialization before coprocessor is over. Going to initialize the coprocessor test
9D	Coprocessor initialized. Going to do any initialization after coprocessor test
9E	Initialization after coprocessor test is complete. Going to check extended keyboard, keyboard ID and num-lock
A2	Going to display any soft errors
A3	Soft error display complete. Going to set keyboard typematic rate
A4	Keyboard typematic rate set. To program memory wait states
A5	Going to enable parity/NMI
A7	NMI and parity enabled. Going to do any initialization required before giving control to optional ROM at E000
A8	Initialization before E000 ROM control over. E000 ROM to get control next
A9	Returned from E000 ROM control. Going to do any initialization required after E000 optional ROM control

Intel D810E2CB Runtime Continued	
AA	Initialization after E000 optional ROM control is over. Going to display the system configuration
AB	Put Int13 module runtime image to shadow
AC	Generate MP for multiprocessor support (if present)
AD	Put CGA Int10 module (if present) in shadow
AE	Uncompress SMBIOS module and init SMBIOS code and form the runtime SMBIOS image in shadow
B1	Going to copy any code to specific area
00	Copying of code to specific area done. Going to give control to Int19 boot loader

Intel D810EMO BIOS

Uncompressed INIT Code Checkpoints

Post Code	Description
D0	NMI is disabled. Onboard keyboard controller and real time clock enabled (if present). Initialization code checksum verification starting
D1	Keyboard controller BAT test, CPU ID saved, and going to 4GB flat mode
D3	Initialize chipset, start memory refresh, & determine mem size
D4	Verify base memory
D5	Initialization code to be copied to segment 0 and control to be transferred to segment 0
D6	Control is in segment 0. Used to check if in recovery mode and to verify main BIOS checksum. If in recovery mode or if main BIOS checksum is wrong, go to checkpoint E0 for recovery. Otherwise, got o checkpoint D7 to give control to main BIOS
D7	Find main BIOS module in ROM image
D8	Uncompress the main BIOS module
D9	Copy main BIOS image to F000 shadow RAM and give control to main BIOS in F000 shadow RAM

Intel D810EMO Continued	
00	Copying of code to specific area done. Going to give control to Int19 boot loader

Intel D810EMO Boot Block Recovery

Post Code	Description
E0	Onboard diskette controller (if any) is initialized. Compressed recovery code is uncompressed at F000:0000 in shadow RAM. Give control to recovery code at F000 in shadow RAM. Initialize interrupt vector tables, system timer, DMA controller, and interrupt controller
E8	Initialize extra (Intel recovery) module
E9	Initialize diskette drive
EA	Try to boot from diskette. If reading of boot sector is successful, give control to boot sector code
EB	Boot from diskette failed; look for ATAPI (LS-120, Zip) devices
EC	Try to boot from ATAPI device. If reading of boot sector is successful, give control to boot sector code
EF	Boot from diskette and ATAPI device failed. Give two beeps. Retry the booting procedure (go to checkpoint E9)

Intel D810EMO Runtime Code

Uncompressed in F000 Shadow RAM

Post Code	Description
03	NMI is disabled. To check soft reset/power on
05	BIOS stack set. Going to disable cache if any
06	POST code to be uncompressed
07	CPU init and CPU data area init to be done
08	CMOS checksum calculation to be done next
0B	Any initialization before keyboard BAT done next

Intel D810EMO Runtime Continued	
0C	Keyboard controller I/B free. To issure the BAT command to the keyboard controller
0E	Any initialization after keyboard controller BAT done next
0F	Keyboard command byte written
10	Going to issue Pin 23, 24 blocking/unblocking command
11	Going to check pressing of <INS>, <END> key during power on
12	To init CMOS if "Init CMOS in every boot" is set or <END> key is pressed. Going to disable DMA and interrupt controllers
13	Video display is disabled and port B is initialized. Chipset init about to begin
14	8254 timer test about to start
19	About to start memory refresh test
1A	Memory refresh line is toggling. Going to check 15 µs On/OFF time
23	To read 8042 input port and disable mega key Green PC feature. Make BIOS cade segment writeable
24	To do any setup before int vector init
25	Interrupt vector initialization to begin. To clear password if necessary
27	Any initialization before setting video mode to be done
28	Going for monochrome mode and color mode setting
2A	Different buses init (system, static, output devices) to start if present
2B	To give control for any setup required before optional ROM check
2C	To look for optional video ROM and give control
2D	To give control to do any processing after video ROM returns control
2E	If EGA/VGA not found then do display memory R/W
2F	EGA/VGA not found. Display memory R/W test about to begin

Intel D810EMO Runtime Continued	
30	Display memory R/W test passed. About to look for the retrace checking
31	Display memory R/W test or retrace checking failed. To do alternate Display memory R/W test
32	Alternate Display memory R/W test passed. To look for the alternate display retrace checking
34	Video display checking over. Display mode set next
37	Display mode set. Going to display power on message
38	Different buses init (input, IPL, general devices) to start if present
39	Display different buses initialization error messages
3A	New cursor position read and saved. To display the Hit <DEL> message
40	To prepare the descriptor tables
42	To enter virtual mode for memory test
43	To enable interrupts for diagnostics mode
44	To initialize data to check memory wrap around at 0:0
45	Data initialized. Going to check for memory wrap around at 0:0 and finding the total system test memory
46	Memory wrap around test done. Memory size calculation over. About to go for writing patterns to test memory.
47	Pattern to be tested written in extended memory. Going to write patterns in base 640KB memory
48	Patterns written in base memory. Going to find out amount of memory below 1M memory
49	Amount of memory below 1M found and verified. Going to find out amount of memory above 1M
4B	Amount of memory above 1M found and verified. Check for soft reset and going to clear memory below 1M for soft reset. (If power on, go to check point # 4E
4C	Memory below 1M cleared. (SOFT RESET) Going to clear memory above 1M
4D	Memory above 1M cleared (SOFT RESET) Going to save the memory size (Go to check point # 52

Intel D810EMO Runtime Continued	
4E	Memory test started. (NOT SOFT RESET) About to display the first 64KB memory size
4F	Memory size display started. This will be updated during memory test. Going for sequential and random memory test
50	Memory testing/initialization below 1MB complete. Going to adjust displayed memory size for relocation shadow
51	Memory size display adjusted due to relocation/shadow. Memory test above 1MB to follow
52	Memory testing/initialization above 1MB complete. Going to save memory size information
53	Memory size information is saved. CPU registers are saved. Going to enter real mode
54	Shutdown successful, CPU in real mode. Going to disable gate A20 line and disable parity/NMI
57	A20 address line, parity/NMI disable successful. Adjust memory size depending on relocation/shadow
58	Memory size adjusted for relocation/shadow. Going to clear hit <DEL> message
59	Hit <DEL> message cleared. <WAIT...> message displayed. About to start DMA and interrupt controller test
60	DMA page register test passed. To do DMA #1 base register test
62	DMA #1 base register test passed. To do DMA #2 base register test
65	DMA #2 base register test passed. To program DMA #1 and #2
66	DMA #1 and #2 programming over. To initialize 8259 interrupt controller
7F	Extended NMI sources enabling is in progress
80	Keyboard test started. Clearing output buffer, checking for stuck key, to issue keyboard reset command
81	Keyboard reset error/stuck key found. To issue keyboard controller interface test command

Intel D810EMO Runtime Continued	
82	Keyboard controller interface test over. To write command byte and init circular buffer
83	Command byte written, global data init done. To check for lock-key
84	Lock key checking over. To check for memory size mismatch with CMOS
85	Memory size check done. To display soft error and check for password or bypass setup
86	Password checked. About to do programming before setup
87	Programming before setup complete. To uncompress SETUP code and execute CMOS setup
88	Returned from CMOS setup program and screen is cleared. About to do programming after setup
89	Programming after setup complete. Going to display power-on screen message
8B	First screen message displayed. <WAIT...> message displayed. PS/2 mouse check and extended BIOS data area allocation to be done
8C	Setup options programming after CMOS setup about to start
8D	Going to hard disk controller reset
8F	Hard disk controller reset done. Floppy setup done next
91	Floppy setup complete. Hard disk setup done next
95	Init of different buses optional ROMs from C800 to start.
96	Going to do any init before C800 optional ROM control
97	Any init before C800 optional ROM control is over. Optional ROM check and control will be done next
98	Optional ROM control is done. About to give control to do any required processing after optional ROM returns control and enable external cache
99	Any initialization required after optional ROM test over. Going to setup timer data area and printer base address
9A	Return after setting timer and printer base addresses. Going to set the RS-232 base address

Intel D810EMO Runtime Continued	
9B	Returned after RS-232 base address. Going to do any initialization before coprocessor test
9C	Required initialization before coprocessor is over. Going to initialize the coprocessor test
9D	Coprocessor initialized. Going to do any initialization after coprocessor test
9E	Initialization after coprocessor test is complete. Going to check extended keyboard, keyboard ID and num-lock
A2	Going to display any soft errors
A3	Soft error display complete. Going to set keyboard typematic rate
A4	Keyboard typematic rate set. To program memory wait states
A5	Going to enable parity/NMI
A7	NMI and parity enabled. Going to do any initialization required before giving control to optional ROM at E000
A8	Initialization before E000 ROM control over. E000 ROM to get control next
A9	Returned from E000 ROM control. Going to do any initialization required after E000 optional ROM control
AA	Initialization after E000 optional ROM control is over. Going to display the system configuration
AB	Put Int13 module runtime image to shadow
AC	Generate MP for multiprocessor support (if present)
AD	Put CGA Int10 module (if present) in shadow
AE	Uncompress SMBIOS module and init SMBIOS code and form the runtime SMBIOS image in shadow
B1	Going to copy any code to specific area
00	Copying of code to specific area done. Going to give control to Int19 boot loader

Intel D815BN BIOS

Uncompressed INIT Code Checkpoints

Post Code	Description
D0	NMI is disabled. Onboard keyboard controller and real time clock enabled (if present). Initialization code checksum verification starting
D1	Keyboard controller BAT test, CPU ID saved, and going to 4GB flat mode
D3	Initialize chipset, start memory refresh, and determine memory size
D4	Verify base memory
D5	Initialization code to be copied to segment 0 and control to be transferred to segment 0
D6	Control is in segment 0. Used to check if in recovery mode and to verify main BIOS checksum. If in recovery mode or if main BIOS checksum is wrong, go to checkpoint E0 for recovery. Otherwise, got o checkpoint D7 to give control to main BIOS
D7	Find main BIOS module in ROM image
D8	Uncompress the main BIOS module
D9	Copy main BIOS image to F000 shadow RAM and give control to main BIOS in F000 shadow RAM

Intel D815BN Boot Block Recovery

Post Code	Description
E0	Onboard diskette controller (if any) is initialized. Compressed recovery code is uncompressed at F000:0000 in shadow RAM. Give control to recovery code at F000 in shadow RAM. Initialize interrupt vector tables, system timer, DMA controller, and interrupt controller
E8	Initialize extra (Intel recovery) module
E9	Initialize diskette drive

Intel D815BN Boot Block Recovery Continued	
EA	Try to boot from diskette. If reading of boot sector is successful, give control to boot sector code
EB	Boot from diskette failed; look for ATAPI (LS-120, Zip) devices
EC	Try to boot from ATAPI device. If reading of boot sector is successful, give control to boot sector code
EF	Boot from diskette and ATAPI device failed. Give two beeps. Retry the booting procedure (go to checkpoint E9)

Intel D815BN Runtime Code

Uncompressed in F000 Shadow RAM

Post Code	Description
03	NMI is disabled. To check soft reset/power on
05	BIOS stack set. Going to disable cache if any
06	POST code to be uncompressed
07	CPU init and CPU data area init to be done
08	CMOS checksum calculation to be done next
0B	Any initialization before keyboard BAT done next
0C	Keyboard controller I/B free. To issure the BAT command to the keyboard controller
0E	Any initialization after keyboard controller BAT to be done next
0F	Keyboard command byte written
10	Going to issue Pin 23, 24 blocking/unblocking command
11	Going to check pressing of <INS>, <END> key during power-on
12	To init CMOS if "Init CMOS in every boot" is set or <END> key is pressed. Going to disable DMA and interrupt controllers
13	Video display is disabled and port B is initialized. Chipset init about to begin
14	8254 timer test about to start

Intel D815BN Runtime Continued	
19	About to start memory refresh test
1A	Memory refresh line is toggling. Going to check 15 µs On/OFF time
23	To read 8042 input port and disable mega key Green PC feature. Make BIOS cade segment writeable
24	To do any setup before int vector init
25	Interrupt vector initialization to begin. To clear password if necessary
27	Any initialization before setting video mode to be done
28	Going for monochrome mode and color mode setting
2A	Different buses init (system, static, output devices) to start if present
2B	To give control for any setup required before optional ROM check
2C	To look for optional video ROM and give control
2D	To give control to do any processing after video ROM returns control
2E	If EGA/VGA not found then do display memory R/W
2F	EGA/VGA not found. Display memory R/W test about to begin
30	Display memory R/W test passed. About to look for the retrace checking
31	Display memory R/W test or retrace checking failed. To do alternate Display memory R/W test
32	Alternate Display memory R/W test passed. To look for the alternate display retrace checking
34	Video display checking over. Display mode set next
37	Display mode set. Going to display power on message
38	Different buses init (input, IPL, general devices) to start if present
39	Display different buses initialization error messages
3A	New cursor position read and saved. To display the Hit <DEL> message

Intel D815BN Runtime Continued	
40	To prepare the descriptor tables
42	To enter virtual mode for memory test
43	To enable interrupts for diagnostics mode
44	To initialize data to check memory wrap around at 0:0
45	Data initialized. Going to check for memory wrap around at 0:0 and finding the total system test memory
46	Memory wrap around test done. Memory size calculation over. About to go for writing patterns to test memory.
47	Pattern to be tested written in extended memory. Going to write patterns in base 640KB memory
48	Patterns written in base memory. Going to find out amount of memory below 1M memory
49	Amount of memory below 1M found and verified. Going to find out amount of memory above 1M
4B	Amount of memory above 1M found and verified. Check for soft reset and going to clear memory below 1M for soft reset. (If power on, go to check point # 4E
4C	Memory below 1M cleared. (SOFT RESET) Going to clear memory above 1M
4D	Memory above 1M cleared (SOFT RESET) Going to save the memory size (Go to check point # 52
4E	Memory test started. (NOT SOFT RESET) About to display the first 64KB memory size
4F	Memory size display started. This will be updated during memory test. Going for sequential and random memory test
50	Memory testing/initialization below 1MB complete. Going to adjust displayed memory size for relocation shadow
51	Memory size display adjusted due to relocation/shadow. Memory test above 1MB to follow
52	Memory testing/initialization above 1MB complete. Going to save memory size information
53	Memory size information is saved. CPU registers are saved. Going to enter real mode

Intel D815BN Runtime Continued	
54	Shutdown successful, CPU in real mode. Going to disable gate A20 line and disable parity/NMI
57	A20 address line, parity/NMI disable successful. Adjust memory size depending on relocation/shadow
58	Memory size adjusted for relocation/shadow. Going to clear hit <DEL> message
59	Hit <DEL> message cleared. <WAIT...> message displayed. About to start DMA and interrupt controller test
60	DMA page register test passed. To do DMA #1 base register test
62	DMA #1 base register test passed. To do DMA #2 base register test
65	DMA #2 base register test passed. To program DMA #1 and #2
66	DMA #1 and #2 programming over. To initialize 8259 interrupt controller
7F	Extended NMI sources enabling is in progress
80	Keyboard test started. Clearing output buffer, checking for stuck key, to issue keyboard reset command
81	Keyboard reset error/stuck key found. To issue keyboard controller interface test command
82	Keyboard controller interface test over. To write command byte and init circular buffer
83	Command byte written, global data init done. To check for lock-key
84	Lock key checking over. To check for memory size mismatch with CMOS
85	Memory size check done. To display soft error and check for password or bypass setup
86	Password checked. About to do programming before setup
87	Programming before setup complete. To uncompress SETUP code and execute CMOS setup
88	Returned from CMOS setup program and screen is cleared. About to do programming after setup

Intel D815BN Runtime Continued	
89	Programming after setup complete. Going to display power-on screen message
8B	First screen message displayed. <WAIT...> message displayed. PS/2 mouse check and extended BIOS data area allocation to be done
8C	Setup options programming after CMOS setup about to start
8D	Going to hard disk controller reset
8F	Hard disk controller reset done. Floppy setup to be done next
91	Floppy setup complete. Hard disk setup done next
95	Init of different buses optional ROMs from C800 to start.
96	Going to do any init before C800 optional ROM control
97	Any init before C800 optional ROM control is over. Optional ROM check and control will be done next
98	Optional ROM control is done. About to give control to do any required processing after optional ROM returns control and enable external cache
99	Any initialization required after optional ROM test over. Going to setup timer data area and printer base address
9A	Return after setting timer and printer base addresses. Going to set the RS-232 base address
9B	Returned after RS-232 base address. Going to do any initialization before coprocessor test
9C	Required initialization before coprocessor is over. Going to initialize the coprocessor test
9D	Coprocessor initialized. Going to do any initialization after coprocessor test
9E	Initialization after coprocessor test is complete. Going to check extended keyboard, keyboard ID and num-lock
A2	Going to display any soft errors
A3	Soft error display complete. Going to set keyboard typematic rate
A4	Keyboard typematic rate set. To program memory wait states

Intel D815BN Runtime Continued	
A5	Going to enable parity/NMI
A7	NMI and parity enabled. Going to do any initialization required before giving control to optional ROM at E000
A8	Initialization before E000 ROM control over. E000 ROM to get control next
A9	Returned from E000 ROM control. Going to do any initialization required after E000 optional ROM control
AA	Initialization after E000 optional ROM control is over. Going to display the system configuration
AB	Put Int13 module runtime image to shadow
AC	Generate MP for multiprocessor support (if present)
AD	Put CGA Int10 module (if present) in shadow
AE	Uncompress SMBIOS module and init SMBIOS code and form the runtime SMBIOS image in shadow
B1	Going to copy any code to specific area
00	Copying of code to specific area done. Going to give control to Int19 boot loader

Intel D815EEA BIOS

Uncompressed INIT Code Checkpoints

Post Code	Description
D0	NMI is disabled. Onboard keyboard controller and real time clock enabled (if present). Initialization code checksum verification starting
D1	Keyboard controller BAT test, CPU ID saved, and going to 4GB flat mode
D3	Initialize chipset, start memory refresh, & determine mem size
D4	Verify base memory
D5	Initialization code to be copied to segment 0 and control to be transferred to segment 0
D6	Control is in segment 0. Used to check if in recovery mode and to verify main BIOS checksum. If in recovery mode or

	if main BIOS checksum is wrong, go to checkpoint E0 for recovery. Otherwise, got o checkpoint D7 to give control to main BIOS
D7	Find main BIOS module in ROM image
D8	Uncompress the main BIOS module
D9	Copy main BIOS image to F000 shadow RAM and give control to main BIOS in F000 shadow RAM

Intel D815EEA Boot Block Recovery

Post Code	Description
E0	Onboard diskette controller (if any) is initialized. Compressed recovery code is uncompressed at F000:0000 in shadow RAM. Give control to recovery code at F000 in shadow RAM. Initialize interrupt vector tables, system timer, DMA controller, and interrupt controller
E8	Initialize extra (Intel recovery) module
E9	Initialize diskette drive
EA	Try to boot from diskette. If reading of boot sector is successful, give control to boot sector code
EB	Boot from diskette failed; look for ATAPI (LS-120, Zip) devices
EC	Try to boot from ATAPI device. If reading of boot sector is successful, give control to boot sector code
EF	Boot from diskette and ATAPI device failed. Give two beeps. Retry the booting procedure (go to checkpoint E9)

Intel D815EEA Runtime Code

Uncompressed in F000 Shadow RAM

Post Code	Description
03	NMI is disabled. To check soft reset/power on
05	BIOS stack set. Going to disable cache if any

Intel D815EEA Runtime Continued	
06	POST code to be uncompressed
07	CPU init and CPU data area init to be done
08	CMOS checksum calculation to be done next
0B	Any initialization before keyboard BAT done next
0C	Keyboard controller I/B free. To issure the BAT command to the keyboard controller
0E	Any initialization after keyboard controller BAT done next
0F	Keyboard command byte written
10	Going to issue Pin 23, 24 blocking/unblocking command
11	Going to check pressing of <INS>,<END> key during power on
12	To init CMOS if "Init CMOS in every boot" is set or <END> key is pressed. Going to disable DMA and interrupt controllers
13	Video display is disabled and port B is initialized. Chipset init about to begin
14	8254 timer test about to start
19	About to start memory refresh test
1A	Memory refresh line is toggling. Going to check 15 µs On/OFF time
23	To read 8042 input port and disable mega key Green PC feature. Make BIOS cade segment writeable
24	To do any setup before int vector init
25	Interrupt vector initialization to begin. To clear password if necessary
27	Any initialization before setting video mode to be done
28	Going for monochrome mode and color mode setting
2A	Different buses init (system, static, output devices) to start if present
2B	Give control for any setup required before optional ROM check
2C	To look for optional video ROM and give control
2D	Give control to do any processing after video ROM returns control

Intel D815EEA Runtime Continued	
2E	If EGA/VGA not found then do display memory R/W
2F	EGA/VGA not found. Display memory R/W test about to begin
30	Display memory R/W test passed. About to look for the retrace checking
31	Display memory R/W test or retrace checking failed. To do alternate Display memory R/W test
32	Alternate Display memory R/W test passed. To look for the alternate display retrace checking
34	Video display checking over. Display mode set next
37	Display mode set. Going to display power on message
38	Different buses init (input, IPL, general devices) to start if present
39	Display different buses initialization error messages
3A	New cursor position read and saved. To display the Hit <DEL> message
40	To prepare the descriptor tables
42	To enter virtual mode for memory test
43	To enable interrupts for diagnostics mode
44	To initialize data to check memory wrap around at 0:0
45	Data initialized. Going to check for memory wrap around at 0:0 and finding the total system test memory
46	Memory wrap around test done. Memory size calculation over. About to go for writing patterns to test memory.
47	Pattern to be tested written in extended memory. Going to write patterns in base 640KB memory
48	Patterns written in base memory. Going to find out amount of memory below 1M memory
49	Amount of memory below 1M found and verified. Going to find out amount of memory above 1M
4B	Amount of memory above 1M found and verified. Check for soft reset and going to clear memory below 1M for soft reset. (If power on, go to check point # 4E

Intel D815EEA Runtime Continued	
4C	Memory below 1M cleared. (SOFT RESET) Going to clear memory above 1M
4D	Memory above 1M cleared (SOFT RESET) Going to save the memory size (Go to check point # 52
4E	Memory test started. (NOT SOFT RESET) About to display the first 64KB memory size
4F	Memory size display started. This is updated during memory test. Going for sequential and random memory test
50	Memory testing/initialization below 1MB complete. Going to adjust displayed memory size for relocation shadow
51	Memory size display adjusted due to relocation/shadow. Memory test above 1MB to follow
52	Memory testing/initialization above 1MB complete. Going to save memory size information
53	Memory size information is saved. CPU registers are saved. Going to enter real mode
54	Shutdown successful, CPU in real mode. Going to disable gate A20 line and disable parity/NMI
57	A20 address line, parity/NMI disable successful. Adjust memory size depending on relocation/shadow
58	Memory size adjusted for relocation/shadow. Going to clear hit <DEL> message
59	Hit <DEL> message cleared. <WAIT...> message displayed. About to start DMA and interrupt controller test
60	DMA page register test passed. To do DMA #1 base register test
62	DMA #1 base register test passed. To do DMA #2 base register test
65	DMA #2 base register test passed. To program DMA #1 & #2
66	DMA #1 and #2 programming over. To initialize 8259 interrupt controller
7F	Extended NMI sources enabling is in progress
80	Keyboard test started. Clearing output buffer, checking for stuck key, to issue keyboard reset command

Intel D815EEA Runtime Continued	
81	Keyboard reset error/stuck key found. To issue keyboard controller interface test command
82	Keyboard controller interface test over. To write command byte and init circular buffer
83	Command byte written, global data init done. To check for lock-key
84	Lock key checking over. To check for memory size mismatch with CMOS
85	Memory size check done. To display soft error and check for password or bypass setup
86	Password checked. About to do programming before setup
87	Programming before setup complete. To uncompress SETUP code and execute CMOS setup
88	Returned from CMOS setup program and screen is cleared. About to do programming after setup
89	Programming after setup complete. Going to display power-on screen message
8B	First screen message displayed. <WAIT...> message displayed. PS/2 mouse check and extended BIOS data area allocation to be done
8C	Setup options programming after CMOS setup about to start
8D	Going to hard disk controller reset
8F	Hard disk controller reset done. Floppy setup to be done next
91	Floppy setup complete. Hard disk setup done next
95	Init of different buses optional ROMs from C800 to start.
96	Going to do any init before C800 optional ROM control
97	Any init before C800 optional ROM control is over. Optional ROM check and control will be done next
98	Optional ROM control is done. About to give control to do any required processing after optional ROM returns control and enable external cache
99	Any initialization required after optional ROM test over. Going to setup timer data area and printer base address

Intel D815EEA Runtime Continued	
9A	Return after setting timer and printer base addresses. Going to set the RS-232 base address
9B	Returned after RS-232 base address. Going to do any initialization before coprocessor test
9C	Required initialization before coprocessor is over. Going to initialize the coprocessor test
9D	Coprocessor initialized. Going to do any initialization after coprocessor test
9E	Initialization after coprocessor test is complete. Going to check extended keyboard, keyboard ID and num-lock
A2	Going to display any soft errors
A3	Soft error display complete. Going to set keyboard typematic rate
A4	Keyboard typematic rate set. To program memory wait states
A5	Going to enable parity/NMI
A7	NMI and parity enabled. Going to do any initialization required before giving control to optional ROM at E000
A8	Initialization before E000 ROM control over. E000 ROM to get control next
A9	Returned from E000 ROM control. Going to do any initialization required after E000 optional ROM control
AA	Initialization after E000 optional ROM control is over. Going to display the system configuration
AB	Put Int13 module runtime image to shadow
AC	Generate MP for multiprocessor support (if present)
AD	Put CGA Int10 module (if present) in shadow
AE	Uncompress SMBIOS module and init SMBIOS code and form the runtime SMBIOS image in shadow
B1	Going to copy any code to specific area
00	Copying of code to specific area done. Going to give control to Int19 boot loader

Intel D815EPEA BIOS

Uncompressed INIT Code Checkpoints

Post Code	Description
D0	NMI is disabled. Onboard keyboard controller and real time clock enabled (if present). Initialization code checksum verification starting
D1	Keyboard controller BAT test, CPU ID saved, and going to 4GB flat mode
D3	Initialize chipset, start memory refresh, and determine memory size
D4	Verify base memory
D5	Initialization code to be copied to segment 0 and control to be transferred to segment 0
D6	Control is in segment 0. Used to check if in recovery mode and to verify main BIOS checksum. If in recovery mode or if main BIOS checksum is wrong, go to checkpoint E0 for recovery. Otherwise, got o checkpoint D7 to give control to main BIOS
D7	Find main BIOS module in ROM image
D8	Uncompress the main BIOS module
D9	Copy main BIOS image to F000 shadow RAM and give control to main BIOS in F000 shadow RAM

Intel D815EPEA Boot Block Recovery

Post Code	Description
E0	Onboard diskette controller (if any) is initialized. Compressed recovery code is uncompressed at F000:0000 in shadow RAM. Give control to recovery code at F000 in shadow RAM. Initialize interrupt vector tables, system timer, DMA controller, and interrupt controller
E8	Initialize extra (Intel recovery) module
E9	Initialize diskette drive

Intel D815EPEA Boot Block Recovery Continued	
EA	Try to boot from diskette. If reading of boot sector is successful, give control to boot sector code
EB	Boot from diskette failed; look for ATAPI (LS-120, Zip) devices
EC	Try to boot from ATAPI device. If reading of boot sector is successful, give control to boot sector code
EF	Boot from diskette and ATAPI device failed. Give two beeps. Retry the booting procedure (go to checkpoint E9)

Intel D815EPEA Runtime Code

Uncompressed in F000 Shadow RAM

Post Code	Description
03	NMI is disabled. To check soft reset/power on
05	BIOS stack set. Going to disable cache if any
06	POST code to be uncompressed
07	CPU init and CPU data area init to be done
08	CMOS checksum calculation to be done next
0B	Any initialization before keyboard BAT done next
0C	Keyboard controller I/B free. To issure the BAT command to the keyboard controller
0E	Any initialization after keyboard controller BAT to be done next
0F	Keyboard command byte written
10	Going to issue Pin 23, 24 blocking/unblocking command
11	Going to check pressing of <INS>, <END> key during power-on
12	To init CMOS if "Init CMOS in every boot" is set or <END> key is pressed. Going to disable DMA and interrupt controllers
13	Video display is disabled and port B is initialized. Chipset init about to begin

Intel D815EPEA Runtime Continued	
14	8254 timer test about to start
19	About to start memory refresh test
1A	Memory refresh line is toggling. Going to check 15 µs On/OFF time
23	To read 8042 input port and disable mega key Green PC feature. Make BIOS cade segment writeable
24	To do any setup before int vector init
25	Interrupt vector initialization to begin. To clear password if necessary
27	Any initialization before setting video mode to be done
28	Going for monochrome mode and color mode setting
2A	Different buses init (system, static, output devices) to start if present
2B	To give control for any setup required before optional ROM check
2C	To look for optional video ROM and give control
2D	To give control to do any processing after video ROM returns control
2E	If EGA/VGA not found then do display memory R/W
2F	EGA/VGA not found. Display memory R/W test about to begin
30	Display memory R/W test passed. About to look for the retrace checking
31	Display memory R/W test or retrace checking failed. To do alternate Display memory R/W test
32	Alternate Display memory R/W test passed. To look for the alternate display retrace checking
34	Video display checking over. Display mode set next
37	Display mode set. Going to display power on message
38	Different buses init (input, IPL, general devices) to start if present
39	Display different buses initialization error messages
3A	New cursor position read and saved. To display the Hit <DEL> message

Intel D815EPEA Runtime Continued	
40	To prepare the descriptor tables
42	To enter virtual mode for memory test
43	To enable interrupts for diagnostics mode
44	To initialize data to check memory wrap around at 0:0
45	Data initialized. Going to check for memory wrap around at 0:0 and finding the total system test memory
46	Memory wrap around test done. Memory size calculation over. About to go for writing patterns to test memory.
47	Pattern to be tested written in extended memory. Going to write patterns in base 640KB memory
48	Patterns written in base memory. Going to find out amount of memory below 1M memory
49	Amount of memory below 1M found and verified. Going to find out amount of memory above 1M
4B	Amount of memory above 1M found and verified. Check for soft reset and going to clear memory below 1M for soft reset. (If power on, go to check point # 4E
4C	Mem below 1M cleared. (SOFT RESET) Going to clear mem above 1M
4D	Memory above 1M cleared (SOFT RESET) Going to save the memory size (Go to check point # 52
4E	Memory test started. (NOT SOFT RESET) About to display the first 64KB memory size
4F	Memory size display started. This will be updated during memory test. Going for sequential and random memory test
50	Memory testing/initialization below 1MB complete. Going to adjust displayed memory size for relocation shadow
51	Memory size display adjusted due to relocation/shadow. Memory test above 1MB to follow
52	Memory testing/initialization above 1MB complete. Going to save memory size information
53	Memory size information is saved. CPU registers are saved. Going to enter real mode

Intel D815EPEA Runtime Continued	
54	Shutdown successful, CPU in real mode. Going to disable gate A20 line and disable parity/NMI
57	A20 address line, parity/NMI disable successful. Adjust memory size depending on relocation/shadow
58	Memory size adjusted for relocation/shadow. Going to clear hit <DEL> message
59	Hit <DEL> message cleared. <WAIT...> message displayed. About to start DMA and interrupt controller test
60	DMA page register test passed. To do DMA #1 base register test
62	DMA #1 base register test passed. To do DMA #2 base register test
65	DMA #2 base register test passed. To program DMA #1 and #2
66	DMA #1 and #2 programming over. To initialize 8259 interrupt controller
7F	Extended NMI sources enabling is in progress
80	Keyboard test started. Clearing output buffer, checking for stuck key, to issue keyboard reset command
81	Keyboard reset error/stuck key found. To issue keyboard controller interface test command
82	Keyboard controller interface test over. To write command byte and init circular buffer
83	Command byte written, global data init done. To check for lock-key
84	Lock key checking over. To check for memory size mismatch with CMOS
85	Memory size check done. To display soft error and check for password or bypass setup
86	Password checked. About to do programming before setup
87	Programming before setup complete. To uncompress SETUP code and execute CMOS setup
88	Returned from CMOS setup program and screen is cleared. About to do programming after setup

Intel D815EPEA Runtime Continued	
89	Programming after setup complete. Going to display power-on screen message
8B	First screen message displayed. <WAIT...> message displayed. PS/2 mouse check and extended BIOS data area allocation to be done
8C	Setup options programming after CMOS setup about to start
8D	Going to hard disk controller reset
8F	Hard disk controller reset done. Floppy setup to be done next
91	Floppy setup complete. Hard disk setup done next
95	Init of different buses optional ROMs from C800 to start.
96	Going to do any init before C800 optional ROM control
97	Any init before C800 optional ROM control is over. Optional ROM check and control will be done next
98	Optional ROM control is done. About to give control to do any required processing after optional ROM returns control and enable external cache
99	Any initialization required after optional ROM test over. Going to setup timer data area and printer base address
9A	Return after setting timer and printer base addresses. Going to set the RS-232 base address
9B	Returned after RS-232 base address. Going to do any initialization before coprocessor test
9C	Required initialization before coprocessor is over. Going to initialize the coprocessor test
9D	Coprocessor initialized. Going to do any initialization after coprocessor test
9E	Initialization after coprocessor test is complete. Going to check extended keyboard, keyboard ID and num-lock
A2	Going to display any soft errors
A3	Soft error display complete. Going to set keyboard typematic rate
A4	Keyboard typematic rate set. To program memory wait states

Intel D815EPEA Runtime Continued	
A5	Going to enable parity/NMI
A7	NMI and parity enabled. Going to do any initialization required before giving control to optional ROM at E000
A8	Initialization before E000 ROM control over. E000 ROM to get control next
A9	Returned from E000 ROM control. Going to do any initialization required after E000 optional ROM control
AA	Initialization after E000 optional ROM control is over. Going to display the system configuration
AB	Put Int13 module runtime image to shadow
AC	Generate MP for multiprocessor support (if present)
AD	Put CGA Int10 module (if present) in shadow
AE	Uncompress SMBIOS module and init SMBIOS code and form the runtime SMBIOS image in shadow
B1	Going to copy any code to specific area
00	Copying of code to specific area done. Going to give control to Int19 boot loader

Intel D820LP BIOS

Uncompressed INIT Code Checkpoints

Post Code	Description
D0	NMI is disabled. Onboard keyboard controller and real time clock enabled (if present). Initialization code checksum verification starting
D1	Keyboard controller BAT test, CPU ID saved, and going to 4GB flat mode
D3	Initialize chipset, start memory refresh, and determine memory size
D4	Verify base memory
D5	Initialization code to be copied to segment 0 and control to be transferred to segment 0

Intel D820LP BIOS Continued	
D6	Control is in segment 0. Used to check if in recovery mode and to verify main BIOS checksum. If in recovery mode or if main BIOS checksum is wrong, go to checkpoint E0 for recovery. Otherwise, got o checkpoint D7 to give control to main BIOS
D7	Find main BIOS module in ROM image
D8	Uncompress the main BIOS module
D9	Copy main BIOS image to F000 shadow RAM and give control to main BIOS in F000 shadow RAM

Intel D820LP Boot Block Recovery

Post Code	Description
E0	Onboard diskette controller (if any) is initialized. Compressed recovery code is uncompressed at F000:0000 in shadow RAM. Give control to recovery code at F000 in shadow RAM. Initialize interrupt vector tables, system timer, DMA controller, and interrupt controller
E8	Initialize extra (Intel recovery) module
E9	Initialize diskette drive
EA	Try to boot from diskette. If reading of boot sector is successful, give control to boot sector code
EB	Boot from diskette failed; look for ATAPI (LS-120, Zip) devices
EC	Try to boot from ATAPI device. If reading of boot sector is successful, give control to boot sector code
EF	Boot from diskette and ATAPI device failed. Give two beeps. Retry the booting procedure (go to checkpoint E9)

Intel D820LP Runtime Code

Uncompressed in F000 Shadow RAM

Post Code	Description
03	NMI is disabled. To check soft reset/power on
05	BIOS stack set. Going to disable cache if any
06	POST code to be uncompressed
07	CPU init and CPU data area init to be done
08	CMOS checksum calculation to be done next
0B	Any initialization before keyboard BAT to be done next
0C	Keyboard controller I/B free. To issure the BAT command to the keyboard controller
0E	Any initialization after keyboard controller BAT to be done next
0F	Keyboard command byte written
10	Going to issue Pin 23, 24 blocking/unblocking command
11	Going to check pressing of <INS>, <END> key during power-on
12	To init CMOS if "Init CMOS in every boot" is set or <END> key is pressed. Going to disable DMA and interrupt controllers
13	Video display is disabled and port B is initialized. Chipset init about to begin
14	8254 timer test about to start
19	About to start memory refresh test
1A	Memory refresh line is toggling. Going to check 15 µs On/OFF time
23	To read 8042 input port and disable mega key Green PC feature. Make BIOS cade segment writeable
24	To do any setup before int vector init
25	Interrupt vector initialization to begin. To clear password if necessary
27	Any initialization before setting video mode to be done

Intel D820LP Runtime Continued	
28	Going for monochrome mode and color mode setting
2A	Different buses init (system, static, output devices) to start if present
2B	To give control for any setup required before optional ROM check
2C	To look for optional video ROM and give control
2D	To give control to do any processing after video ROM returns control
2E	If EGA/VGA not found then do display memory R/W
2F	EGA/VGA not found. Display memory R/W test about to begin
30	Display memory R/W test passed. About to look for the retrace checking
31	Display memory R/W test or retrace checking failed. To do alternate Display memory R/W test
32	Alternate Display memory R/W test passed. To look for the alternate display retrace checking
34	Video display checking over. Display mode set next
37	Display mode set. Going to display power on message
38	Different buses init (input, IPL, general devices) to start if present
39	Display different buses initialization error messages
3A	New cursor position read and saved. To display the Hit <DEL> message
40	To prepare the descriptor tables
42	To enter virtual mode for memory test
43	To enable interrupts for diagnostics mode
44	To initialize data to check memory wrap around at 0:0
45	Data initialized. Going to check for memory wrap around at 0:0 and finding the total system test memory
46	Memory wrap around test done. Memory size calculation over. About to go for writing patterns to test memory.

Intel D820LP Runtime Continued	
47	Pattern to be tested written in extended memory. Going to write patterns in base 640KB memory
48	Patterns written in base memory. Going to find out amount of memory below 1M memory
49	Amount of memory below 1M found and verified. Going to find out amount of memory above 1M
4B	Amount of memory above 1M found and verified. Check for soft reset and going to clear memory below 1M for soft reset. (If power on, go to check point # 4E
4C	Memory below 1M cleared. (SOFT RESET) Going to clear memory above 1M
4D	Memory above 1M cleared (SOFT RESET) Going to save the memory size (Go to check point # 52
4E	Memory test started. (NOT SOFT RESET) About to display the first 64KB memory size
4F	Memory size display started. This will be updated during memory test. Going for sequential and random memory test
50	Memory testing/initialization below 1MB complete. Going to adjust displayed memory size for relocation shadow
51	Memory size display adjusted due to relocation/shadow. Memory test above 1MB to follow
52	Memory testing/initialization above 1MB complete. Going to save memory size information
53	Memory size information is saved. CPU registers are saved. Going to enter real mode
54	Shutdown successful, CPU in real mode. Going to disable gate A20 line and disable parity/NMI
57	A20 address line, parity/NMI disable successful. Adjust memory size depending on relocation/shadow
58	Memory size adjusted for relocation/shadow. Going to clear hit <DEL> message
59	Hit <DEL> message cleared. <WAIT...> message displayed. About to start DMA and interrupt controller test

Intel D820LP Runtime Continued	
60	DMA page register test passed. To do DMA #1 base register test
62	DMA #1 base register test passed. To do DMA #2 base register test
65	DMA #2 base register test passed. To program DMA #1 and #2
66	DMA #1 and #2 programming over. To initialize 8259 interrupt controller
7F	Extended NMI sources enabling is in progress
80	Keyboard test started. Clearing output buffer, checking for stuck key, to issue keyboard reset command
81	Keyboard reset error/stuck key found. To issue keyboard controller interface test command
82	Keyboard controller interface test over. To write command byte and init circular buffer
83	Command byte written, global data init done. To check for lock-key
84	Lock key checking over. to check for memory size mismatch with CMOS
85	Memory size check done. to display soft error and check for password or bypass setup
86	Password checked. About to do programming before setup
87	Programming before setup complete. To uncompress SETUP code and execute CMOS setup
88	Returned from CMOS setup program and screen is cleared. About to do programming after setup
89	Programming after setup complete. Going to display power-on screen message
8B	First screen message displayed. <WAIT...> message displayed. PS/2 mouse check and extended BIOS data area allocation to be done
8C	Setup options programming after CMOS setup about to start
8D	Going to hard disk controller reset

Intel D820LP Runtime Continued	
8F	Hard disk controller reset done. Floppy setup to be done next
91	Floppy setup complete. Hard disk setup done next
95	Init of different buses optional ROMs from C800 to start.
96	Going to do any init before C800 optional ROM control
97	Any init before C800 optional ROM control is over. Optional ROM check and control will be done next
98	Optional ROM control is done. About to give control to do any required processing after optional ROM returns control and enable external cache
99	Any initialization required after optional ROM test over. Going to setup timer data area and printer base address
9A	Return after setting timer and printer base addresses. Going to set the RS-232 base address
9B	Returned after RS-232 base address. Going to do any initialization before coprocessor test
9C	Required initialization before coprocessor is over. Going to initialize the coprocessor test
9D	Coprocessor initialized. Going to do any initialization after coprocessor test
9E	Initialization after coprocessor test is complete. Going to check extended keyboard, keyboard ID and num-lock
A2	Going to display any soft errors
A3	Soft error display complete. Going to set keyboard typematic rate
A4	Keyboard typematic rate set. To program memory wait states
A5	Going to enable parity/NMI
A7	NMI and parity enabled. Going to do any initialization required before giving control to optional ROM at E000
A8	Initialization before E000 ROM control over. E000 ROM to get control next
A9	Returned from E000 ROM control. Going to do any initialization required after E000 optional ROM control

Intel D820LP Runtime Continued	
AA	Initialization after E000 optional ROM control is over. Going to display the system configuration
AB	Put Int13 module runtime image to shadow
AC	Generate MP for multiprocessor support (if present)
AD	Put CGA Int10 module (if present) in shadow
AE	Uncompress SMBIOS module and init SMBIOS code and form the runtime SMBIOS image in shadow
B1	Going to copy any code to specific area
00	Copying of code to specific area done. Going to give control to Int19 boot loader

Intel SE440BX BIOS

Uncompressed INIT Code Checkpoints

Post Code	Description
02	Verify real mode
03	Disable non-maskable interrupts (NMI)
04	Get processor type
06	Initialize system hardware
08	Initialize chipset with initial POST values
09	Set IN POST flag
0A	Initialize CPU registers
0B	Enable CPU cache
0C	Initialize caches to initial POST values
0E	Initialize I/O component
0F	Initialize the local bus IDE
10	Initialize power management
11	Load alternate registers with initial POST values new
12	Restore control word during warm boot
13	Initialize PCI bus mastering devices
14	Initialize keyboard controller

Intel SE440BX BIOS Continued	
16	BIOS ROM checksum
17	Initialize cache before memory auto size
18	8254 timer initialization
1A	8237 DMA controller initialization
1C	Reset programmable interrupt controller
20	Test DRAM refresh
22	Test keyboard controller
24	Set ES segment register to 4GB
26	Enable A20 line
28	Auto size DRAM
29	Initialize POST memory manager
2A	Clear 512KB base RAM
2C	RAM failure on address line xxxx
2E	RAM failure on data bits xxxx of low byte of memory bus
2F	Enable cache before system BIOS shadow
30	RAM failure on data bits xxxx of high byte of memory bus
32	Test CPU bus-clock frequency
33	Initialize POST dispatch manager
34	Test CMOS RAM
35	Initialize alternate chipset registers
36	Warm start shut down
37	Reinitialize the chipset (motherboard only)
38	Shadow system BIOS ROM
39	Reinitialize the cache (motherboard only)
3A	Auto size cache
3C	Configure advanced chipset registers
3D	Load alternate registers with CMOS values new
40	Set initial CPU speed new
42	Initialize interrupt vectors
44	Initialize BIOS interrupts

Intel SE440BX BIOS Continued	
45	POST device initialization
46	Check ROM copyright notice
47	Initialize manager for PCI option ROMs
48	Check video configuration against CMOS RAM data
49	Initialize PCI bus and devices
4A	Initialize all video adapters in system
4B	Display Quiet Boot screen
4C	Shadow video BIOS ROM
4E	Display BIOS copyright notice
50	Display CPU type and speed
51	Initialize EISA motherboard
52	Test keyboard
54	Set key click if enabled
56	Enable keyboard
58	Test for unexpected interrupts
59	Initialize POST display service
5A	Display prompt "Press F2 to enter SETUP"
5B	Disable CPU cache
5C	Test RAM between 512KB and 640KB
60	Test extended memory
62	Test extended memory address lines
64	Jump to User Patch 1
66	Configure advanced cache registers
67	Initialize multiprocessor APIC
68	Enable external and processor caches
69	Setup System Management Mode (SMM) area
6A	Display external L2 cache size
6C	Display shadow-area message
6E	Display possible high address for UMB recovery
70	Display error messages

Intel SE440BX BIOS Continued	
72	Check for configuration errors
74	Test real-time clock
76	Check for keyboard errors
7A	Test for key lock on
7C	Set up hardware interrupt vectors
7E	Initialize coprocessor if present
80	Disable onboard Super I/O ports and IRQ's
81	Late POST device initialization
82	Detect and install external RS232 ports
83	Configure non-MCD IDE controllers
84	Detect and install external parallel ports
85	Initialize PC-compatible PnP ISA devices
86	Reinitialize onboard I/O ports
87	Configure motherboard configurable devices
88	Initialize BIOS Data Area
89	Enable non-maskable interrupts (NMI)
8A	Initialize extended BIOS data area
8B	Test and initialize PS/2 mouse
8C	Initialize diskette controller
8F	Determine number of ATA drives
90	Initialize hard-disk controllers
91	Initialize local-bus hard-disk controllers
92	Jump to User Patch 2
93	Build MPTABLE for multiprocessor boards
94	Disable A20 address line (Rel. 5.1 and earlier)
95	Install CD-ROM for boot
96	Clear huge ES segment register
97	Fix up multiprocessor table
98	Search for option ROMs

Intel SE440BX BIOS Continued	
99	Check for SMART drive
9A	Shadow option ROMs
9C	Setup power management
9E	Enable hardware interrupts
A0	Set time of day
A2	Check key lock
A4	Initialize typematic rate
A8	Erase F2 prompt
AA	Scan for F2 key stroke
AC	Enter SETUP
AE	Clear IN POST flag
B0	Check for errors
B2	POST done - prepare to boot operating system
B4	One short beep before boot
B5	Terminate Quiet Boot
B6	Check password (optional)
B8	Clear global descriptor table
B9	Clean up all graphics
BA	Initialize DMI parameters
BB	Initialize PnP Option ROMs
BC	Clear parity checkers
BD	Display Multi Boot menu
BE	Clear screen
BF	Check virus and backup reminders
C0	Try to boot with Int19h
C1	Initialize POST Error Manager (PEM)
C2	Initialize error logging
C3	Initialize error display function
C4	Initialize system error handler

Intel SE440BX BIOS Continued	
E0	Initialize the chipset
E1	Initialize the bridge
E2	Initialize the processor
E3	Initialize system timer
E4	Initialize system I/O
E5	Check force recovery boot
E6	Checksum BIOS ROM
E7	Go to BIOS
E8	Set huge segment
E9	Initialize multiprocessor
EA	Initialize OEM specific code
EB	Initialize PIC and DMA
EC	Initialize memory type
ED	Initialize memory size
EE	Shadow boot block
EF	System memory test
F0	Initialize interrupt vectors
F1	Initialize runtime clock
F2	Initialize video
F4	Initialize boot
F5	Clear huge segment
F6	Boot to mini-DOS
F7	Boot to full DOS

Intel SR440BX BIOS

Uncompressed INIT Code Checkpoints

Post Code	Description
D0	NMI is disabled. Onboard KBC, RTC enabled (if present). Init code checksum verification starting

Intel SR440BX BIOS Continued	
D1	Keyboard controller BAT test, CPU ID saved, and going to 4GB flat mode
D3	Do necessary chipset initialization, start memory refresh, and do memory sizing
D4	Verify base memory
D5	init code to be copied to segment 0 and control to be transferred to segment 0
D6	Control is in segment 0. To check recovery mode and verify main BIOS checksum. If either it is recovery mode or main BIOS checksum is bad, go to check point E0 for recovery else go to check point D7 for giving control to main BIOS.
D7	Find main BIOS module in ROM image
D8	Uncompress the main BIOS module
D9	Copy main BIOS image to F000 shadow RAM and give control to amin BIOS in F000 shadow RAM

Intel SR440BX Boot Block Recovery

Post Code	Description
E0	Onboard floppy controller (if any) is initialized. Compressed recovery code is uncompressed in F000:0000 in shadow RAM and give control to recovery code in F000 shadow RAM. Initialize interrupt vector tables, initialize system timer, initialize DMA controller and interrupt controller
E8	Initialize extra (Intel Recovery) Module
E9	Initialize floppy drive
EA	Try to boot from floppy
EB	Booting from floppy failed, look for ATAPI (LS120, Zip) devices
EC	Try to boot from ATAPI. If reading boot sector is successful, give control to boot sector code

Intel SR440BX Boot Block Recovery Continued	
EF	Booting from floppy failed and ATAPI device failed. Give two beeps. Retry the booting procedure again (go back to check point E9)

Intel SR440BX Runtime Code

Uncompressed in F000 Shadow RAM

Post Code	Description
03	NMI is disabled. To check soft reset/power on
05	BIOS stack set. Going to disable cache if any
06	POST code to be uncompressed
07	CPU init and CPU data area init to be done
08	CMOS checksum calculation to be done next
0B	Any initialization before keyboard BAT to be done next
0C	Keyboard controller I/B free. To issure the BAT command to the keyboard controller
0E	Any initialization after keyboard controller BAT to be done next
0F	Keyboard command byte written
10	Going to issue Pin 23, 24 blocking/unblocking command
11	Going to check pressing of <INS>, <END> key during power-on
12	To init CMOS if "Init CMOS in every boot" is set or <END> key is pressed. Going to disable DMA and interrupt controllers
13	Video display is disabled and port B is initialized. Chipset init about to begin
14	8254 timer test about to start
19	About to start memory refresh test
1A	Memory refresh line is toggling. Going to check 15 µs On/OFF time
23	To read 8042 input port and disable mega key Green PC feature. Make BIOS cade segment writeable

Intel SR440BX Runtime Continued	
24	To do any setup before int vector init
25	Interrupt vector initialization to begin. To clear password if necessary
27	Any initialization before setting video mode to be done
28	Going for monochrome mode and color mode setting
2A	Different buses init (system, static, output devices) to start if present
2B	To give control for any setup required before optional ROM check
2C	To look for optional video ROM and give control
2D	To give control to do any processing after video ROM returns control
2E	If EGA/VGA not found then do display memory R/W
2F	EGA/VGA not found. Display memory R/W test about to begin
30	Display memory R/W test passed. About to look for the retrace checking
31	Display memory R/W test or retrace checking failed. To do alternate Display memory R/W test
32	Alternate Display memory R/W test passed. To look for the alternate display retrace checking
34	Video display checking over. Display mode set next
37	Display mode set. Going to display power on message
38	Different buses init (input, IPL, general devices) to start if present
39	Display different buses initialization error messages
3A	New cursor position read and saved. To display the Hit <DEL> message
40	To prepare the descriptor tables
42	To enter virtual mode for memory test
43	To enable interrupts for diagnostics mode
44	To initialize data to check memory wrap around at 0:0

Intel SR440BX Runtime Continued	
45	Data initialized. Going to check for memory wrap around at 0:0 and finding the total system test memory
46	Memory wrap around test done. Memory size calculation over. About to go for writing patterns to test memory.
47	Pattern to be tested written in extended memory. Going to write patterns in base 640KB memory
48	Patterns written in base memory. Going to find out amount of memory below 1M memory
49	Amount of memory below 1M found and verified. Going to find out amount of memory above 1M
4B	Amount of memory above 1M found and verified. Check for soft reset and going to clear memory below 1M for soft reset. (If power on, go to check point # 4E
4C	Memory below 1M cleared. (SOFT RESET) Going to clear memory above 1M
4D	Memory above 1M cleared (SOFT RESET) Going to save the memory size (Go to check point # 52
4E	Memory test started. (NOT SOFT RESET) About to display the first 64KB memory size
4F	Memory size display started. This will be updated during memory test. Going for sequential and random memory test
50	Memory testing/initialization below 1MB complete. Going to adjust displayed memory size for relocation shadow
51	Memory size display adjusted due to relocation/shadow. Memory test above 1MB to follow
52	Memory testing/initialization above 1MB complete. Going to save memory size information
53	Memory size information is saved. CPU registers are saved. Going to enter real mode
54	Shutdown successful, CPU in real mode. Going to disable gate A20 line and disable parity/NMI
57	A20 address line, parity/NMI disable successful. Adjust memory size depending on relocation/shadow

Intel SR440BX Runtime Continued	
58	Memory size adjusted for relocation/shadow. Going to clear hit <DEL> message
59	Hit <DEL> message cleared. <WAIT...> message displayed. About to start DMA and interrupt controller test
60	DMA page register test passed. To do DMA #1 base register test
62	DMA #1 base register test passed. To do DMA #2 base register test
65	DMA #2 base register test passed. To program DMA #1 and #2
66	DMA #1 and #2 programming over. To initialize 8259 interrupt controller
7F	Extended NMI sources enabling is in progress
80	Keyboard test started. Clearing output buffer, checking for stuck key, to issue keyboard reset command
81	Keyboard reset error/stuck key found. To issue keyboard controller interface test command
82	Keyboard controller interface test over. To write command byte and init circular buffer
83	Command byte written, global data init done. To check for lock-key
84	Lock key checking over. To check for memory size mismatch with CMOS
85	Memory size check done. To display soft error and check for password or bypass setup
86	Password checked. About to do programming before setup
87	Programming before setup complete. To uncompress SETUP code and execute CMOS setup
88	Returned from CMOS setup program and screen is cleared. About to do programming after setup
89	Programming after setup complete. Going to display power-on screen message
8B	First screen message displayed. <WAIT...> message displayed. PS/2 mouse check and extended BIOS data area allocation to be done

Intel SR440BX Runtime Continued	
8C	Setup options programming after CMOS setup about to start
8D	Going to hard disk controller reset
8F	Hard disk controller reset done. Floppy setup to be done next
91	Floppy setup complete. Hard disk setup done next
95	Init of different buses optional ROMs from C800 to start.
96	Going to do any init before C800 optional ROM control
97	Any init before C800 optional ROM control is over. Optional ROM check and control will be done next
98	Optional ROM control is done. About to give control to do any required processing after optional ROM returns control and enable external cache
99	Any initialization required after optional ROM test over. Going to setup timer data area and printer base address
9A	Return after setting timer and printer base addresses. Going to set the RS-232 base address
9B	Returned after RS-232 base address. Going to do any initialization before coprocessor test
9C	Required initialization before coprocessor is over. Going to initialize the coprocessor test
9D	Coprocessor initialized. Going to do any initialization after coprocessor test
9E	Initialization after coprocessor test is complete. Going to check extended keyboard, keyboard ID and num-lock
A2	Going to display any soft errors
A3	Soft error display complete. Going to set keyboard typematic rate
A4	Keyboard typematic rate set. To program memory wait states
A5	Going to enable parity/NMI
A7	NMI and parity enabled. Going to do any initialization required before giving control to optional ROM at E000

Intel SR440BX Runtime Continued	
A8	Initialization before E000 ROM control over. E000 ROM to get control next
A9	Returned from E000 ROM control. Going to do any initialization required after E000 optional ROM control
AA	Initialization after E000 optional ROM control is over. Going to display the system configuration
AB	Put Int13 module runtime image to shadow
AC	Generate MP for multiprocessor support (if present)
AD	Put CGA Int10 module (if present) in shadow
AE	Uncompress SMBIOS module and init SMBIOS code and form the runtime SMBIOS image in shadow
B1	Going to copy any code to specific area
00	Copying of code to specific area done. Going to give control to Int19 boot loader

Intel JN440BX BIOS

Uncompressed INIT Code Checkpoints

Post Code	Description
02	Verify real mode
03	Disable non-maskable interrupt (NMI)
04	Get processor type
06	Initialize system hardware
08	Initialize chipset with initial POST values
09	Set IN POST flag
0A	Initialize processor registers
0B	Enable processor cache
0C	Initialize caches to initial POST values
0E	Initialize I/O component
0F	Initialize the local bus IDE
10	Initialize power management

Intel JN440BX BIOS Continued	
11	Load alternate registers with initial POST values new
12	Restore processor control word during warm boot
13	Initialize PCI bus mastering devices
14	Initialize keyboard controller
16	BIOS ROM checksum
17	Initialize cache before memory auto size
18	8254 timer initialization
1A	8237 DMA controller initialization
1C	Reset programmable interrupt controller
20	Test DRAM refresh
22	Test keyboard controller
24	Set ES segment register to 4GB
26	Enable A20 line
28	Auto size DRAM
29	Initialize POST memory manager
2A	Clear 512KB base RAM
2C	RAM failure on address line xxxx
2E	RAM failure on data bits xxxx of low byte of memory bus
2F	Enable cache before system BIOS shadow
30	RAM failure on data bits xxxx of high byte of memory bus
32	Test processor bus-clock frequency
33	Initialize POST dispatch manager
34	Test CMOS RAM
35	Initialize alternate chipset registers
36	Warm start shut down
37	Reinitialize the chipset (motherboard only)
38	Shadow system BIOS ROM
39	Reinitialize the cache (motherboard only)
3A	Auto size cache
3C	Configure advanced chipset registers

Intel JN440BX BIOS Continued	
3D	Load alternate registers with CMOS values new
40	Set initial processor speed new
42	Initialize interrupt vectors
44	Initialize BIOS interrupts
45	POST device initialization
46	Check ROM copyright notice
47	Initialize manager for PCI option ROMs
48	Check video configuration against CMOS RAM data
49	Initialize PCI bus and devices
4A	Initialize all video adapters in system
4B	Display Quiet Boot screen
4C	Shadow video BIOS ROM
4E	Display BIOS copyright notice
50	Display processor type and speed
51	Initialize EISA motherboard
52	Test keyboard
54	Set key click if enabled
56	Enable keyboard
58	Test for unexpected interrupts
59	Initialize POST display service
5A	Display prompt "Press F2 to enter "SETUP"
5B	Disable processor cache
5C	Test RAM between 512 and 640KB
60	Test extended memory
62	Test extended memory address lines
64	Jump to UserPatch1
66	Configure advanced cache registers
67	Initialize multiprocessor APIC
68	Enable external and processor caches
69	Setup System Management Mode (SMM) area

Intel JN440BX BIOS Continued	
6A	Display external L2 cache size
6C	Display shadow area message
6E	Display possible high address for UMB recovery
70	Display error messages
72	Check for configuration errors
74	Test real-time clock
76	Check for keyboard errors
7A	Test for key lock on
7C	Setup hardware interrupt vectors
7E	Disable onboard Super I/O ports and IRQs
81	Late POST device initialization
82	Detect and install external RS232 ports
83	Configure non-MCD IDE controllers
84	Detect and install external parallel ports
85	Initialize PC compatible PnP ISA devices
86	Reinitialize onboard I/O ports
87	Configure motherboard configurable devices
88	Initialize BIOS Data Area
89	Enable non-maskable interrupts (NMI)
8A	Initialize extended BIOS data area
8B	Test and initialize PS/2 mouse
8C	Initialize diskette controller
8F	Determine number of ATA drives
90	Initialize hard disk controllers
91	Initialize local bus hard disk controllers
92	Jump to UserPatch2
93	Build MPTABLE for multiprocessor boards
94	Disable A20 address line
95	Install CD-ROM for boot
96	Clear huge ES segment register

Intel JN440BX BIOS Continued	
97	Fix up multiprocessor table
98	Search for option ROMs
99	Check for SMART drive
9A	Shadow option ROMs
9C	Setup power management
9E	Enable hardware interrupts
9F	Determine number of ATA and SCSI drives
A0	Set time of day
A2	Check key lock
A4	Initialize typematic rate
A8	Erase F2 prompt
AA	Scan for F2 key stroke
AC	Enter SETUP
AE	Clear IN POST flag
B0	Check for errors
B2	POST done - prepare to boot operating system
B4	One short beep before boot
B5	Terminate Quiet Boot
B6	Check password (optional)
B8	Clear global descriptor table
B9	Clean up all graphics
BA	Initialize DMI parameters
BB	Initialize PnP Option ROMs
BC	Clear parity checkers
BD	Display Multi Boot menu
BE	Clear screen (optional)
BF	Check virus and backup reminders
C0	Try to boot with Int19h
C1	Initialize POST Error Manager (PEM)

Intel JN440BX BIOS Continued	
C2	Initialize error logging
C3	Initialize error display function
C4	Initialize system error handler
E0	Initialize the chipset
E1	Initialize the bridge
E2	Initialize the processor
E3	Initialize system timer
E4	Initialize system I/O
E5	Check force recovery boot
E6	Checksum BIOS ROM
E7	Go to BIOS
E8	Set huge segment
E9	Initialize multiprocessor
EA	Initialize OEM special code
EB	Initialize PIC and DMA
EC	Initialize memory type
ED	Initialize memory speed
EE	Shadow boot block
EF	System memory test
F0	Initialize interrupt vectors
F1	Initialize runtime clock
F2	Initialize video
F3	Initialize beeper
F4	Initialize boot
F5	Clear huge segment
F6	Boot to mini-DOS
F7	Boot to full DOS

Intel LB440GX / LB440GX BIOS

Post Code	Description
02	Verify real mode
12	Restore processor control word during warm boot (only occurs on warm boot)
24	Set ES segment register to 4GB
04	Get processor type
06	Initialize system hardware
18	8254 timer initialization
08	Initialize PCI set registers with initial POST values
C4	Initialize system flags in CMOS
11	Load alternate registers with initial POST values
0E	Initialize I/O
0C	Initialize caches to initial POST values
16	BIOS ROM checksum
17	Turn cache off
28	Auto size DRAM
2A	Clear 512KB base RAM
2C	RAM failure on address line xxxx
2E	RAM failure on data bits xxxx of low byte of memory bus (1st 4Meg)
2F	Initialize L2 cache if enabled in CMOS
38	Shadow system BIOS ROM
20	Test DRAM refresh
29	Post Memory Manager initialization (PMM)
33	Post Dispatch Manager initialization
34	Test CMOS
C1	Post error manager initialization
09	Set IN POST flag
0A	Initialize processor registers and processor microcode

Intel LB440GX / LB440GX BIOS Continued	
3A	Auto size cache
0B	Enable processor cache
0F	Initialize local bus IDE (not used anymore but here for Phoenix standard)
10	Initialize Power Mgmnt (APM not used in L440GX+)
14	Initialize keyboard controller
1A	8237 DMA controller initialization
1C	Reset programmable interrupt controller (PIC)
22	Test 8742 keyboard controller
32	Read processor bus-clock frequency & compute boot processor speed
67	Initialize and register via SMM through APIC bus
69	Initialize SMI handler for all processors
00	Wait for secondary processor to execute init SMI handler
F4	Exit SMI handler (secondary processor executed halt in SMI)
3C	Configure advanced PCI set registers and reset coprocessor
3D	Load alternate registers with CMOS values
42	Initialize interrupt vectors
46	Check ROM copyright notice
45	Initialize all pre-PnP devices
49	Initialize PCI bus and devices (read ESCD & allocate resources)
48	Check video configuration against CMOS (VGA or MDA)
4A	Initialize all video adapters in system
4C	Shadow video BIOS ROM
24	Put processor in big real mode (flat mode memory addressing - up to 4GB)
59	Post display manager initialization (video screen error codes now visible)
22	Reset and test keyboard first try (only warm reset)
52	Reset and test keyboard controller (both warm and cold reset)

Intel LB440GX / LB440GX BIOS Continued	
54	Set key click if enabled
76	Enable keyboard
58	Test for unexpected interrupts
4B	Quiet Boot start (not used in L440GX+)
4E	Display copyright notice
50	Display processor(s) type and speed
51	EISA init (not used in L440GX+)
5A	Display prompt "Press F2 to enter SETUP"
5B	Disable processor L1 cache for memory test
5C	Test RAM between 512KB and 640KB
60	Test extended memory (4MB to top of memory)
62	Test extended memory address lines
64	Jump to UserPatch1
66	Configure advanced cache registers
68	Enable external and processor caches
6A	Display external cache size
6C	Display shadow message
6E	Display non-disposable segments
70	Display error messages to video
72	Check for configuration errors
74	Test real time clock
7C	Setup hardware interrupt vectors
7E	Test coprocessor if present
80	Not used
88	Initialize BIOS Data Area, time-outs for detecting parallel, serial and HDD controller. Clear CMOS shutdown flag
8A	Initialize Extended BIOS Data Area
81	Late POST core initialization of devices
87	Configure MCD devices
85	Initialize and detect PC compatible PnP ISA devices (parallel, serial, etc.)

Intel LB440GX / LB440GX BIOS Continued	
82	Not used
84	Clear interrupts from COM port detection
86	Console redirection initialized
83	Configure onboard hard disk controller
89	Enable NMI
8C	Initialize floppy controller
90	Initialize and detect hard disks
8B	Detect & test for mouse and auxiliary device on keyboard controller
95	Install CD-ROM for boot
92	Jump to UserPatch2
C5	Initialize GPNV areas in DMI
98	Search for option ROMs. One long, two short beeps on checksum failure of an option ROM
93	Scan for User Flash ROMs. MP Table initialization (wake up secondary processor and halt it)
9C	Setup Power Management (not used)
9D	Enable security
9E	Enable hardware interrupts
A0	Set time of day
A2	Check key lock
A4	Initialize typematic rate
C2	Initialize DMI tables
C3	Log post errors with POST error manager and to SEL in BMC. Update VID bits and memory presence to BMC. Display and FRB errors (watchdog time-outs, bits or processor failures)
A8	Erase F2 prompt
AA	Scan for F2 keystroke
AC	Initialize EMP port if selected. Remove COM2 from BDA if EMP is enabled. Enter SETUP
AE	Clear IN POST flag

Intel LB440GX / LB440GX BIOS Continued	
B0	Turn on secure boot if enabled (secure front panel, blank video, floppy write protect). Check for errors
B2	POST done - prepare to boot Operating System
B4	One short beep before boot
B5	Display Quiet Boot (not used)
BE	Clear screen
B6	Check password (optional)
BC	Clear parity checkers
BA	Not used
B7	ACPI config (table config in memory and BDA)
BD	Display Multi Boot menu if ESC is hit
BF	Display system config summary (if enabled in CMOS)
8F	Get total # of hard drives and put in BDA
91	Program IDE hard drives (timing, PIO modes, etc...)
9F	Save total # of hard drives (SCSI and ATA) in BDA
97	Fix up MP table (checksum)
99	Check SMART hard drive
C7	Prepare to boot to OS. Clean up graphics & PMM areas
C0	Try to boot with Int19h. Return to video mode 3, disable PMM, return to real mode, disable gate A20, clears system memory, resets stack, invokes Int19h
D0	Interrupt handler error
D2	Unknown interrupt error
D4	Pending interrupt error
D6	Initialize option ROM error
D8	Shutdown error
DA	Extended Block Move
DC	Shutdown 10 error

Intel NA440BX / N440BX BIOS

Post Code	Description
02	Verify real mode
12	Restore processor control word during warm boot (only occurs on warm boot)
24	Set ES segment register to 4GB
04	Get processor type
06	Initialize system hardware
18	8254 timer initialization
08	Initialize PCI set registers with initial POST values
C4	Initialize system flags in CMOS
11	Load alternate registers with initial POST values
0E	Initialize I/O
0C	Initialize caches to initial POST values
16	BIOS ROM checksum
17	Turn off cache
28	Auto size DRAM
2A	Clear 512KB base RAM
2C	RAM failure on address line xxxx
2E	RAM failure on data bits xxxx of low byte of memory bus (first 4 meg)
2F	Initialize L2 cache if enabled in CMOS
38	Shadow system BIOS ROM
20	Test DRAM refresh
29	Post Memory Manager initialization (PMM)
33	Post Dispatch Manager initialization
34	Test CMOS
C1	Post error manager initialization
09	Set IN POST flag
0A	Initialize processor registers and CPU microcode

Intel NA440BX / N440BX BIOS Continued	
3A	Auto size cache
0B	Enable processor cache
0F	Initialize the local bus IDE
10	Initialize Power Management (APM not used in Nightshade)
14	Initialize keyboard controller
1A	8237 DMA controller initialization
1C	Reset Programmable Interrupt Controller
22	Test 8742 Keyboard Controller
32	Read processor bus-clock frequency and compute boot processor speed
67	Initialize and register other CPU via SMM through APIC bus
69	Initialize SMI handler for all processors
00	Wait for secondary processor to execute init SMI handler
F4	Exit SMI handler (secondary processor executed halt in SMI)
3C	Configure advanced PCI set registers and reset coprocessor
3D	Load alternate registers with CMOS values
42	Initialize interrupt vectors
46	Check ROM copyright notice
45	Initialize all pre-PnP devices
49	Initialize PnP bus and devices (also read ESCD and allocate resources)
48	Check video configuration against CMOS (VGA or MDA)
4A	Initialize all video adapters in system
4C	Shadow video BIOS ROM
24	Put CPU in big real mode (flat mode memory addressing - up to 4GB)
59	Post display manager initialization (video screen error codes now visible)
22	Reset and test keyboard first try (only warm reset)

Intel NA440BX / N440BX BIOS Continued	
52	Reset and test keyboard controller (both warm and cold reset)
54	Set key click if enabled
76	Enable keyboard
58	Test for unexpected interrupts
4B	Quiet Boot start (not used in N440BX)
4E	Display copyright notice
50	Display CPU(s) type and speed
51	EISA initialized (not used in N440BX)
5A	Display prompt "Press F2 to enter SETUP"
5B	Disable CPU L1 cache for memory test
5C	Test RAM between 512KB and 640KB
60	Test extended memory (4MB to top of memory)
62	Test extended memory address lines
64	Jump to UserPatch1
66	Configure advanced cache registers
68	Enable external and processor caches
6A	Display external cache size
6C	Display shadow message
6E	Display non-disposable segments
70	Display error messages to video
72	Check for configuration errors
74	Test real time clock
7C	Setup hardware interrupt vectors
7E	Test coprocessor if present
80	Not used
88	Initialize BIOS Data Area, time-outs for detecting parallel, serial and HDD controller. Clear CMOS shutdown flag
8A	Initialize Extended BIOS Data Area
81	Late POST core initialization
87	Configure MCD devices

Intel NA440BX / N440BX BIOS Continued	
85	Initialize and detect PC compatible PnP ISA devices (serial, parallel, etc.)
82	Not used
84	Clear interrupts from COM port detection
86	Console redirection initialized
83	Configure onboard hard disk controller
89	Enable NMI
8C	Initialize floppy controller
90	Initialize and detect hard disks
8B	Detect and test for Mouse or Auxiliary device on keyboard controller
95	Install CD-ROM for boot
92	Jump to UserPatch2
C5	Initialize GPNV areas of DMI
98	Search for option ROMs. One long, two short beeps for checksum failure of an option ROM
93	Scan for User flash ROMs. MP Table initialization (wake up secondary processor and halt it)
9C	Setup Power Management (not used)
9D	Enable security
9E	Enable hardware interrupts
A0	Set time of day
A2	Check key lock
A4	Initialize typematic rate
C2	Initialize DMI tables
C3	Log POST errors with POST Error Manager and to SEL in BMC. Update VID bits and memory presence to BMC. Display any FRB errors (watchdog time-outs, bist or CPU failures)
A8	Erase F2 prompt
AA	Scan for F2 keystroke
AC	Initialize EMP port if selected. Remove COM2 from BDA of EMP is enabled. Enter SETUP

Intel NA440BX / N440BX BIOS Continued	
AE	Clear IN POST flag
B0	Turn on secure boot if enabled (secure front panel, blank video, floppy write protect). Check for errors
B2	POST done - prepare to boot Operating System
B4	One short beep before boot
B5	Display Quiet Boot (not used)
BE	Clear screen
B6	Check password (optional)
BC	Clear parity checkers
BA	Not used
B7	ACPI configuration (table configuration in memory and BDA)
BD	Display Multi Boot menu if ESC is hit
BF	Display system configuration summary (if enabled in CMOS)
8F	Get total # of hard drives and put in BDA
91	Program IDE hard drives (timing, PIO modes, etc.)
9F	Save total # of hard drives (SCSI and ATA) in BDA
97	Fix up MP Table (checksum)
99	Check SMART hard drive
C7	Prepare to boot OS, clean up graphics and PMM areas
C0	Try to boot Int19h. Return to video mode 3, disable PMM, return to real mode, disable gate A20, clear system memory, reset stack, invoke Int19h

Intel RC440BX BIOS

Uncompressed INIT Code Checkpoints

Post Code	Description
D0	NMI is Disabled. Onboard KBC, RTC enabled (if present). Init code Checksum verification starting
D1	Keyboard controller BAT test, CPU ID saved, going to 4GB flat mode.

Intel RC440BX BIOS Continued	
D3	Do necessary chipset initialization, start memory refresh, do Memory sizing.
D4	Verify base memory.
D5	Init code to be copied to segment 0 and control to be transferred to segment 0.
D6	Control is in segment 0. To check recovery mode and verify main BIOS checksum. If either it is recovery mode or main BIOS checksum is bad, go to check point E0 for recovery else go to check point D7 for giving control to main BIOS.
D7	Find main BIOS module in ROM image
D8	Uncompress the main BIOS module.
D9	Copy main BIOS image to F000 shadow RAM and give control to main BIOS in F000 shadow RAM.

Intel RC440BX Boot Block Recovery

Post Code	Description
E0	Onboard Floppy Controller (if any) is initialized. Compressed recovery code is uncompressed in F000:0000 in Shadow RAM and give control to recovery code in F000 Shadow RAM. Initialize interrupt vector tables, initialize system timer, initialize DMA controller, interrupt controller.
E8	Initialize extra (Intel Recovery) Module.
E9	Initialize floppy drive
EA	Try to boot from floppy. If reading of boot sector is successful, give control to boot sector code.
EB	Booting from floppy failed, look for ATAPI (LS120, Zip) devices.
EC	Try to boot from ATAPI. If reading of boot sector is successful, give control to boot sector code.
EF	Booting from floppy and ATAPI device failed. Give two beeps. Retry the booting procedure again (go to check point E9).

Intel RC440BX Runtime Code

Uncompressed in F000 Shadow RAM

Post Code	Description
03	NMI is disabled. The check soft reset/power-on
05	BIOS stack set. Going to disable cache if any
06	POST code to be uncompressed
07	CPU Init and CPU data area Init to be done
08	CMOS checksum calculation to be done next
0B	Any initialization before keyboard BAT to be done
0C	KB controller I/B free. To issue the BAT command to keyboard controller
0E	Any initialization after KB controller BAT to be done next
0F	Keyboard command byte to be written
10	Going to issue Pin 23, 24 blocking/unblocking command
11	Going to check pressing of (INS>, <END> key during power on
12	To Init CMOS if "Init CMOS in every boot" is set or <END> key is pressed. Going to disable DMA and Interrupt controllers
13	Video display is disabled and port-B is initialized. Chipset init about to begin
14	8254 timer test about to start
19	About to start memory refresh test
1A	Memory refresh line is toggling. Going to check 15µs ON/OFF time
23	To read 8042 input port and disable mega key Green PC feature. Make BIOS code segment writeable
24	To do any setup before Int vector init
25	Interrupt vector initialization to begin. To clear password if necessary
27	Any initialization before setting video mode to be done
28	Going for monochrome mode and color mode setting

Intel RC440BX Runtime Continued	
2A	Different buses init (system, static, output devices) to start if present
2B	To give control for any setup required before optional video ROM check
2C	To look for optional video ROM and give control
2D	To give control to any processing after video ROM returns control
2E	If EGA/VGA not found then do display memory R/W test
2F	EGA/VGA not found. Display memory R/W test about to begin
30	Display memory R/W test passed. About to look for the retrace checking
31	Display memory R/W test and retrace checking failed. To do alternate Display memory R/W test
32	Alternate Display memory R/W test passed. To look for the alternate display retrace checking
34	Video display checking over. Display mode to be set next
37	Display mode set. Going to display the power on message
38	Different buses init (input, IPL, general devices) to start if present
39	Display different buses initialization error messages
3A	New cursor position read and saved. To display the hit <DEL> message
40	To prepare the descriptor tables
42	To enter in virtual mode for memory test
43	To enable interrupts for diagnostic mode
44	To initialize data to check memory wrap around at 0:0
45	Data initialized. Going to check for memory wrap around at 0:0 and finding the total system memory size
46	Memory wrap around test done. Memory size calculation over. About to go for writing patterns to teat memory
47	Pattern to be tested written in extended memory. Going to write patterns in base 540K memory

Intel RC440BX Runtime Continued	
48	Patterns written in base memory. Going to find out amount of memory below 1MB memory
49	Amount of memory below 1MB found and verified. Going to find out amount of memory above 1MB
4B	Amount of memory above 1MB found and verified. Check for soft reset and going to clear memory below 1MB for soft reset
4C	Memory below 1MB cleared. Going to clear memory above 1MB
4D	Memory above 1MB cleared. Going to save the memory size
4E	Memory test started. About to display the first 64K memory size
4F	Memory size display started. This will be updated during the memory test. Going for sequential and random memory test
50	Memory testing/initialization below 1MB complete. Going to adjust displayed memory size for reallocation/shadow
51	Memory size display adjusted due to reallocation/shadow. Memory test above 1MB to follow
52	Memory testing/initialization above 1MB complete. Going to save memory size information
53	Memory size information is saved. CPU registers are saved. Going to enter real mode
54	Shutdown successful, CPU in real mode. Going to disable gate A20 line and disable parity/NMI
57	A20 address line, parity/NMI disable successful. Going to adjust memory size depending on reallocation/shadow
58	Memory size adjusted for reallocation/shadow. Going to clear Hit <DEL> message
59	Hit <DEL> message cleared. <WAIT...> message displayed. About to start DMA and interrupt controller test
60	DMA page register test passed. To do DMA #1 base register test
62	DMA #1 base register test passed. To do DMA #2 base register test

Intel RC440BX Runtime Continued	
65	DMA #2 base register test passed. To program DMA unit 1 and 2
66	DMA unit 1 and 2 programming over. To initialize 8259 interrupt controller
7F	Extended NMI (sources enabling is in progress
80	Keyboard test started. Clearing output buffer, checking for stuck key, to issue keyboard reset command.
81	Keyboard reset error/stuck key found. To issue keyboard controller interface test command
82	Keyboard controller interface test over. To write command byte and init circular buffer
83	Command byte written, global data init done. To check for lock-key
84	Lock-key checking over. To check for memory size mismatch with CMOS
85	Memory size check done. To display soft error and check for password or bypass setup
86	Password checked. About to do programming before setup
87	Programming before setup complete. To uncompress SETUP code and execute CMOS setup
88	Returned from CMOS setup program and screen is cleared. About to do programming after setup
89	Programming after setup complete. Going to display power on screen message
8B	First screen message displayed. <WAIT> message displayed. PS/2 mouse check and extended BIOS data area allocation to be done
8C	Setup options programming after CMOS setup about to start
8D	Going for hard disk controller reset
8F	Hard disk controller reset done. Floppy setup to be done next
91	Floppy setup complete. Hard disk setup done next
95	Init of different buses optional ROMs from C800 to start
96	Going to do any init before C800 optional ROM control

Intel RC440BX Runtime Continued	
97	Any init before C800 optional ROM control is over. Optional ROM check and control will be done next
98	Optional ROM control is done. About to give control to do any required processing after optional ROM returns control and enable external cache
99	Any initialization required after optional ROM test over. Going to setup timer data area and printer base address
9A	Return after setting timer and printer base address. Going to set the RS-232 base address
9B	Returned after RS-232 base address. Going to do any initialization before coprocessor test
9C	Required initialization before coprocessor is over. Going to initialize the coprocessor next
9D	Coprocessor initialized. Going to do any initialization after coprocessor test
9E	Initialization after coprocessor test is complete. Going to check extended keyboard, keyboard ID and num-lock
A2	Going to display and soft errors
A3	Soft error display complete. Going to set keyboard typematic rate
A4	Keyboard typematic rate set. To program memory wait states
A7	NMI and parity enabled. Going to do any initialization required before giving control to optional ROM at E000
A8	Initialization before E000 ROM control over. E000 ROM to get control next
A9	Returned from E000 ROM control. Going to do any initialization required after E000 optional ROM control
AA	Initialization after E000 optional ROM control is over. Going to display the system configuration
AB	Put INT13 module runtime image to shadow
AC	Generate MP for multiprocessor support (if present)
AD	Put CGA INT10 module (if present) in shadow
AE	Uncompress SMBIOS module and init SMBIOS code and form the runtime SMBIOS image in shadow

Intel RC440BX Runtime Continued	
B1	Going to copy any code to specific area
00	Copying of code to specific area done. Going to give control to INT19 boot loader

Phoenix BIOS Plus Version 1.0

Post Code	Diag. Sect.	Description
01	2.2	CPU Register Test
02	2.6	CMOS Read/Write Error
03	4.2	BIOS ROM Checksum Error
04	3.2	PIT Failure
05	5.7	DMA Initialization Error
06	5.7	DMA Page Register Read/Write Error
08	5.0	RAM Refresh Failure
09	5.0	Test First 64KB RAM
0A	5.0	First 64KB Failure, RAM Chip or Data Line
0B	5.0	First 64KB Parity Logic Failure
0C	5.0	First 64KB, Address Line Failure
0D	5.0	First 64KB Parity Error
10	5.0	First 64KB RAM Failure, Bit 0
11	5.0	First 64KB RAM Failure, Bit 1
12	5.0	First 64KB RAM Failure, Bit 2
13	5.0	First 64KB RAM Failure, Bit 3
14	5.0	First 64KB RAM Failure, Bit 4
15	5.0	First 64KB RAM Failure, Bit 5
16	5.0	First 64KB RAM Failure, Bit 6
17	5.0	First 64KB RAM Failure, Bit 7
18	5.0	First 64KB RAM Failure, Bit 8
19	5.0	First 64KB RAM Failure, Bit 9
1A	5.0	First 64KB RAM Failure, Bit A

Phoenix BIOS Plus Version 1.0 Continued		
1B	5.0	First 64KB RAM Failure, Bit B
1C	5.0	First 64KB RAM Failure, Bit C
1D	5.0	First 64KB RAM Failure, Bit D
1E	5.0	First 64KB RAM Failure, Bit E
1F	5.0	First 64KB RAM Failure, Bit F
20	5.7	DMA Slave Register Failure
21	5.7	DMA Master Register Failure
22	3.1	Failure of Master Interrupt Mask Register
23	3.1	Failure of Slave Interrupt Mask Register
25	3.0	Load Interrupt Vectors
27	8.1	Keyboard Controller Failure
28	2.6	CMOS Checksum
29	2.6	Checking CMOS Configuration
2B	7.4	Video Memory Error
2C	7.0	Video Initialization Error
2D	7.0	Screen Retrace Test Failure
2E	7.3	Search for Video ROM
30	7.3	Start Video ROM
31	7.1	Mono Monitor Test
32	7.2	Color Monitor Test: 40-Column
33	7.2	Color Monitor Test: 80-Column
34	3.2	Tick Timer Interrupt
35	2.6, 5.2	Shutdown Failure
36	5.3	A-20 Gate Error
37	3.0	Protected Mode Unexpected Interrupt
38	5.2	RAM Address Error, 01000-0A000
39	5.0	RAM Address Error, 10000-FFFFF
3A	3.2	Counter 2 Timer Chip Failure
3B	2.5	Time-Of-Day Clock Stopped
3C	6.2	Serial Port Test

Phoenix BIOS Plus Version 1.0 Continued		
3D	6.3	Parallel Port Test
41	2.0	System Board Select Bad
42	2.7	Extended CMOS Error

Phoenix PCI BIOS

Post Code	Diag. Sect.	Description
02	2.6, 5.2	Shutdown in Protected Mode
04	2.2, 2.6	Update CMOS CPU Data (Cold Boot only)
06	2.5, 5.7	Reset DMA Registers and RTC
08	2.4	Initialize Chipset
0A	2.7	Set POST Flag
0C	2.4	Initialize I/O Registers
0E	5.0	Initialize External Cache
10-14	8.1	Verify 8742 Keyboard Controller
16	4.2	Verify BIOS ROM Checksum
18	3.2	Initialize PITs
1A	5.7	Initialize DMA
1C	3.1	Initialize PIC
20	5.0	Test DRAM Refresh
22	8.1	Keyboard Controller Self-Test
24	2.2	Set ES Segment Register to 4GB
26	5.3	Enable A-20 Line
2A	5.0	Clear First 64KB RAM
2C	5.0	Test RAM Address Lines
2E	5.0	Test First 64KB RAM
30, 32	2.2	Verify CPU Speed
34	2.5, 2.6	Verify CMOS Checksum and RTC
36-3A	5.0	Auto-Size External Cache
3C	5.0	Configure External Cache

Phoenix PCI BIOS Continued		
3E	8.0	Read Keyboard Configuration
40	2.6	Set Power-Up Speed per CMOS
42	3.0	Initialize Interrupt Vectors 0-77h
44	3.0	Initialize Interrupt vectors 0-20h
46	4.2	Check Copyright Message Checksum
48	7.0	Check Video Configuration
4A	7.0	Initialize Video Adapters
4C-4E	4.0, 7.0	Display Copyright Message
50	7.0	Display CPU Type and Speed
52	8.0	Keyboard Self-test
54	8.0	Initialize Keystroke Clicker
56	8.0	Enable Keyboard
58	3.0	Check for Unexpected Interrupts
5A	7.0	Display “Press F2 to Enter Setup”
5C	5.0	Size and Test Available Memory
5E	5.0	Base Memory Address Test
60	5.0	Size and Test Extended Memory
62	5.0	Test RAM Addressing
68	2.2	Enable Cache
6A	2.2	Display Cache Size
6C	5.5	Display BIOS Shadow Status
6E	4.0	Display BIOS Starting Segment/Offset
70	9.0	Check for Error Flags
72	9.0	Check for Configuration Errors
74	2.5	Test RTC
76	8.0, 9.0	Check and Display Keyboard Errors
78	8.0	Check for Stuck Keys
7A	8.3	Enable Key Lock
7C	3.0	Set Hardware Interrupt Vectors
7E	2.3	Test Coprocessor

Phoenix PCI BIOS Continued		
80, 82	6.2	Install RS232 Ports
84	6.3	Install Parallel Ports
86, 88	2.4	Initialize Timeout and Reset Flags
8A	2.7, 6.6	Initialize Mouse and Ext. BIOS Data Area
8C	6.5	Initialize Floppy
8E	6.4	Detect Hard Drive Type
90	6.4	Initialize Hard Drive
92, 94	5.3	Disable A-20 Line
96, 98	4.0	Scan for ROM BIOS Extensions
9E	3.0	Enable Hardware Interrupts
A0	2.5	Set Time Of Day
A2	8.1	Set Num lock Indicator
A4	8.1	Initialize Typematic Rate
A6	5.4	Initialize Hard Drive Auto-Park
A8	7.0	Erase F2 Prompt
AA	8.0	Scan for F2 Keystroke
AC	2.6	Check for Setup
AE	2.6	Clear CMOS Flags
B0	9.0	Check for POST Errors
B2	2.4	Set POST-Complete Flag
B4	6.6	Emit One Beep
B6	4.3	Check for Password
B8	2.4	Clear Global Descriptor Table
BA	7.0	Initialize Screen-Saver
BC	5.0	Clear Parity Error Latch
BE	7.0	Clear Screen
C0	4.1	Attempt Int.19 Boot
D0-D2	3.0	Check for Interrupts
D4	3.0	Clear Pending Interrupts
D6-DA	5.0	Return from Extended Block Move

Phoenix PCI BIOS, UMC Chipset

Post Code	Diag. Sect.	Description
02	5.2	Verify Real Mode
04	2.2	Get CPU type
06	2.1	Initialize System Hardware
08	2.4	Initialize Chipset Registers
09	2.4	Set POST Flag
0A	2.2	Initialize CPU Registers
0C	2.2	Initialize Cache
0E	6.6	Initialize I/O
10	1.0	Initialize APM
11	2.4	Load Alternate Registers
12	10.0	User Patch 0
14	8.1	Initialize Keyboard Controller
16	4.2	BIOS ROM Checksum
18	3.2	Initialize 8254 PIT
1A	5.7	Initialize 8237 DMA Controller
1C	3.1	Reset PIC
20	5.0	Test DRAM Refresh
22	8.1	Test 8742 Keyboard Controller
24	2.2	Set ES Segment Register
26	5.3	Enable A-20 Line
28	5.0	Auto-Size DRAM
2A	5.0	Clear Base 512KB RAM
2C	5.0	Test Base 512KB Address Lines
2E	5.0	Test Base 512KB RAM
30	5.0	Test BASE RAM Address Memory
32	2.5	Test CPU Clock Frequency
34	2.6	Test CMOS RAM
35	2.4	Test Chipset Registers

Phoenix PCI BIOS, UMC Chipset Continued		
36	2.6	Test Check Resume
37	2.4	Reinitialize Chipset
38	5.5	Shadow BIOS ROM
39	2.2, 5.0	Reinitialize Cache
3A	5.0	Auto-Size Cache
3C	2.4	Configure Advanced Chipset Registers
3D	2.4, 2.6	Load Alternate Registers from CMOS
3E	8.1	Read Hardware Config of Keyboard Controller
40	2.5	Set Initial CPU Speed
42	3.0	Initialize Interrupt Vectors
44	3.0	Initialize BIOS Interrupts
46	4.0	Check ROM Copyright
47	5.4	Initialize PCI Option ROM Manager
48	7.0	Verify Video Configuration
49	2.1	Initialize PCI Bus and Devices
4A	7.0	Initialize Video Adapters
4C	5.5	Shadow Video BIOS ROM
4E	4.0	Display Copyright Notice
50	2.2	Display CPU Type and Speed
52	8.0	Test Keyboard
54	8.0	Set Key Click (if enabled)
56	8.0	Enable Keyboard
58	3.0	Test for Unexpected Interrupts
5A	7.0	Display “Press F2 to Enter Setup”
5C	5.0	Test RAM, 512-640KB
5E	5.0	Test Base Memory
60	5.0	Test Expanded Memory
62	5.0	Test Extended Memory
64	10.0	User Patch 1
66	5.0	Configure Advanced Cache Registers

Phoenix PCI BIOS, UMC Chipset Continued		
68	2.2	Enable External and CPU Registers
69	2.1	Set Up APM
6A	5.0	Display External Cache Size
6C	5.5	Display Shadow Message
6E	2.2	Display Non-Disposable Segments
70	9.0	Display Error Messages
72	9.0	Check for Configuration Messages
74	2.5	Test RTC
76	8.0	Check for Keyboard Errors
7A	8.3	Enable Key Lock
7C	3.0	Set Up Hardware Interrupt Vectors
7E	2.3	Test Coprocessor
80	6.6	Disable Onboard I/O Ports
82	6.2	Install External RS232-C Ports
84	6.3	Install External Parallel Ports
86	6.6	Reinitialize Onboard I/O Ports
88	5.5	Initialize BIOS Data Areas
8A	5.5	Initialize Extended BIOS Data Area
8C	6.5	Initialize Floppy Controller
8E	6.4	Configure Hard Drive
90	6.4	Initialize Hard Drive Controller
91	6.4	Initialize Local-Bus HD Controller
92	10.0	User Patch 2
94	5.3	Disable A-20 Line
96	2.4	Clear Huge ES Segment Register
98	5.4	Search for Option ROMs
9A	5.5	Shadow Option ROMs
9C	1.0	Set Up Power Management
9E	3.0	Enable Hardware Interrupts
A0	2.5	Set Time Of Day

Phoenix PCI BIOS, UMC Chipset Continued		
A2	8.3	Check Key Lock
A4	8.0	Initialize Typematic Rate
A8	7.0	Erase F2 Prompt
AA	8.0	Scan for F2 Keystroke
AC	2.6	Enter Setup
AE	2.4	Clear In-POST Flag
B0	9.0	Check for Errors
B2	4.1	POST Complete
B4	6.6	Emit One Beep
B6	4.3	Check Password
B8	2.4	Clear Global Descriptor Table
BC	5.0	Clear Parity Checkers
BE	7.0	Clear Screen
C0	4.1	Attempt Int.19 Boot
D0	3.0	Interrupt Handler Error
D2	3.0	Unknown Interrupt Error
D4	3.0	Pending-Interrupt Error
D6	5.4	Error Initializing Option ROM
D8	2.6, 5.2	Shutdown Error
DA	5.0	Extended Block Move
DC	2.6	Shutdown 10 Error

Phoenix ISA / EISA / MCA Version 3.07

Post Code	Diag. Sect.	Description
01	2.2	CPU Register Test
02	2.6	CMOS Write/Read Test
03	4.2	ROM BIOS Checksum
04	3.2	PIT Test
05	5.7	DMA Initialization

Phoenix ISA / EISA / MCA Version 3.07 Continued		
06	5.7	DMA page Register
08	5.1	RAM Refresh Verification
09	5.1	First 64k RAM Test
0A	5.1	First 64k RAM Data Line
0B	5.1	First 64k RAM Parity
0C	5.1	Address Line First 64k RAM
0D	5.1	Parity Bad First 64K RAM
10	5.1	Bit 0 First 64K RAM Bad
11	5.1	Bit 1 First 64K RAM Bad
12	5.1	Bit 2 First 64K RAM Bad
13	5.1	Bit 3 First 64K RAM Bad
14	5.1	Bit 4 First 64K RAM Bad
15	5.1	Bit 5 First 64K RAM Bad
16	5.1	Bit 6 First 64K RAM Bad
17	5.1	Bit 7 First 64K RAM Bad
18	5.1	Bit 8 First 64K RAM Bad
19	5.1	Bit 9 First 64K RAM Bad
1A	5.1	Bit 10 First 64K RAM Bad
1B	5.1	Bit 11 First 64K RAM Bad
1C	5.1	Bit 12 First 64K RAM Bad
1D	5.1	Bit 13 First 64K RAM Bad
1E	5.1	Bit 14 First 64K RAM Bad
1F	5.1	Bit 15 First 64K RAM Bad
20	5.7	Slave DMA Register Bad
21	5.7	Master DMA Register Bad
22	3.1	Master PIC Register Bad
23	3.1	Slave PIC Register Bad
25	3.1, 5.4	Interrupt Vector Loading
27	8.1	Keyboard Controller Test
28	2.6	CMOS Power And Checksum

Phoenix ISA / EISA / MCA Version 3.07 Continued		
29	2.6	CMOS Validation
2B	7.0	Screen Initialization Bad
2C	7.0	Screen Retrace Test Bad
2D	7.3	Search For Video ROM
2E	7.3	Screen Video ROM
30	7.0	Screen Operable
30	7.0	Screen Running With ROM
31	7.1	Monochrome Monitor Operable
32	7.2	Color (40 Column) Operable
33	7.2	Color (80 Column) Operable
34	2.6, 3.2	Timer Tick Interrupt Test
35	2.6, 8.1	Shutdown Test
36	5.2	Gate A20 Bad
37	8.1	Unexpected Interrupt
38	5.1	Extended RAM Test
3A	3.2	Interval Timer Channel 2
3B	2.5	Time-Of-Day Clock
3C	6.2	Serial Port Test
3D	6.3	Parallel Port Test
3E	2.3	Math Coprocessor Test
41	2.0	System Board Select Bad
42	2.7	Extended CMOS RAM Bad

Phoenix BIOS Version 4.0

Post Code	Diag. Sect.	Description
02	5.2	Verify Real Mode
04	2.2	Get CPU Type
06	2.4, 5.4	System Hardware Initialization
08	2.4	Init. Chipset with Initial POST Values

Phoenix BIOS Version 4.0 Continued		
09	2.4	Set Initial POST Values in POST Flag
0A	2.2	CPU Register Initialization
0C	5.6	Init. Cache With Initial POST Values
0E	2.1	I/O Initialization
10	2.4	Power Management Initialization
11	2.4	Initial POST Values to Alt. Registers
12	2.4	User Batch 0
14	8.1	Keyboard Controller Initialization
16	4.2	BIOS ROM Checksum
18	3.2	8254 Timer Initialization
1A	5.7	8237 DMA Controller Initialization
1C	3.1	Reset PIC
20	5.1	DRAM Refresh Test
22	8.1	8742 Keyboard Controller Test
24	2.4	Set ES Segment to Register to 4 GB
28	5.1	Auto size DRAM
2A	5.1	Clear 512k Base RAM
2C	5.1	512k Base Address Lines Test
2E	5.1	512k Base Memory Test
32	2.5	CPU Bus Clock Frequency Test
37	2.4	Reinitialize the Chipset
38	5.5	Shadow System BIOS ROM
39	5.6	Reinitialize the Cache
3A	5.6	Autosize Cache
3C	2.7	Configure Advanced Chipset Registers
3D	2.7	CMOS Values to Alternate Registers
40	2.4	Set Initial CPU Speed
42	2.7	Interrupt Vectors Initialization
44	2.4, 4.0	BIOS Interrupts Initialization
46	4.0	Check ROM Copyright Notice

Phoenix BIOS Version 4.0 Continued		
47	5.4	PCI Options ROMs Initialization
48	2.7, 7.0	Check Video Config. Against CMOS
49	2.1	Initialize PCI Bus and Devices
4A	7.0	Video Initialization
4C	5.5	Shadow Video BIOS ROM
4E	7.0	Display Copyright Notice
50	7.0	Display CPU Type And Speed
52	8.1	Keyboard Test
54	8.1	Set Key Click
56	8.1	Keyboard Enable
58	3.1	Unexpected Interrupts Test
5A	5.7, 7.0	Display "Press F2 To Enter SETUP"
5C	5.1	512k to 640k RAM Test
60	5.1	Expanded Memory Test
62	5.1	Extended Memory Address Lines Test
64	2.7	User Batch 1
66	2.7	Configure Advanced Cache Registers
68	5.6	External/CPU Cache Enable
6A	5.6, 7.0	Display External Cache Size
6C	7.0	Display Shadow Message
6E	7.0	Display Non-Disposable Segments
70	7.0	Display Error Messages
72	2.7	Check for Configuration Errors
74	2.5	Real-Time Clock Test
76	8.1	Check for Keyboard Errors
7C	3.1, 5.4	Set Up Hardware Interrupt Vectors
7E	2.3	NPU Test
80	6.1	Disable Onboard I/O Ports
82	6.2	Detect/Install External RS232 Ports
84	6.3	Detect/Install External Parallel Ports

Phoenix BIOS Version 4.0 Continued		
86	6.1	Re-Initialize Onboard I/O Ports
88	5.5	BIOS Data Area Initialization
8A	5.5	Extended BIOS Data Area Init.
8C	6.5	Floppy Controller Initialization
90	6.4	Hard-Disk Controller Initialization
91	6.4	Local-Bus HD Controller Init.
92	2.7	User Batch 2
94	5.3	Disable A20 Address Line
96	2.2, 2.7	Clear 4 GB ES Segment Register
98	5.4	Search for Option ROMs
9A	5.5	Shadow Option ROMs
9C	2.4	Set Up Power Management
9E	3.1, 5.4	Hardware Interrupts Enable
A0	2.5	Set Time Of Day
A2	8.3	Key Lock Test
A8	7.0	Erase F2 Prompt
AA	8.1	Scan For F2 Key Stroke
AC	2.6, 7.0	Enter SETUP
AE	2.6	Clear POST Flag
B0	2.6	Check for Errors
B2	4.1	Prepare to Boot Operating System
B4	2.6	One Beep
B6	4.3	Password Check
B8	2.7	Clear Global Descriptor Table
BC	2.6	Clear Parity Checkers
BE	7.0	Clear Screen
BF	2.7	Virus/Backup Reminder Check
C0	4.1	Boot with INT 19
D0	4.1	Interrupt Handler Error
D2	6.4, 6.5	Unknown Interrupt Error

Phoenix BIOS Version 4.0 Continued		
D4	6.4, 6.5	Pending Interrupt Error
D6	2.7, 5.4	Option ROM Error Initialization
D8	2.7, 8.1	Shutdown Error
DA	5.1	Extended Block Move
DC	2.7	Shutdown I/O Error
E2	2.4	Chipset Initialization
E3	5.1	Refresh Counter Initialization
E4	2.7	Forced Flash Check
E5	5.4	HW Status of ROM Check
E6	4.0	BIOS ROM OK Test
E7	5.1	RAM Test
E8	2.4	OEM Initialization
E9	3.1	PIC Initialization
EA	4.1	Read In Bootstrap Code
EB	2.1, 3.1	Vector Initialization
EC	4.0	Boot the Flash Program
ED	4.1	Boot Device Initialization
EE	4.1	Boot Code Read OK

Phoenix Version 4 Release 6.0

Post Code	Diag. Sect.	Description
02	5.2	Verify Real Mode
03	2.2, 3.0	Disable Non-maskable Interrupt (NMI)
04	2.2	Get CPU Type
06	2.4, 5.4	System Hardware Initialization
08	2.4	Init. Chipset with Initial POST Values
09	2.4	Set Initial POST Values in POST Flag
0A	2.2	CPU Register Initialization
0B	2.2, 5.6	Enable CPU Cache

Phoenix Version 4 Release 6.0 Continued		
0C	5.6	Init. Cache With Initial POST Values
0E	2.1	I/O Component Initialization
0F	2.1	Initialize Local Bus IDE
10	2.4	Power Management Initialization
11	2.4	Initial POST Values to Alt. Registers
12	2.4	Restore CPU Control Word (in warm boot)
14	8.1	Keyboard Controller Initialization
16	4.2	BIOS ROM Checksum
18	3.2	8254 Timer Initialization
1A	5.7	8237 DMA Controller Initialization
1C	3.1	Reset PIC
20	5.1	DRAM Refresh Test
22	8.1	8742 Keyboard Controller Test
24	2.4	Set ES Segment to Register to 4 GB
28	5.1	Auto size DRAM
29	5.0	Initialize POST Memory Manager
2A	5.1	Clear 512k Base RAM
2C	5.1	RAM Address Failure
2E	5.1	RAM Data Failure, Low Byte
2F	5.6	Enable Cache Prior to BIOS Shadowing
30	5.1	RAM Data Failure, High Byte
32	2.5	CPU Bus Clock Frequency Test
33	6.0	Initialize Phoenix Dispatch Manager
36	2.4	Warm Start Shut Down
38	5.5	Shadow System BIOS ROM
3A	5.6	Autosize Cache
3C	2.7	Configure Advanced Chipset Registers
3D	2.7	CMOS Values to Alternate Registers
42	2.7	Interrupt Vectors Initialization
45	6.1	POST Device Initialization

Phoenix Version 4 Release 6.0 Continued		
46	4.0	Check ROM Copyright Notice
48	2.7, 7.0	Check Video Config. Against CMOS
49	2.1	Initialize PCI Bus and Devices
4A	7.0	Initialize Video Adapters
4B	2.6	Quiet Boot Start (optional)
4C	5.5	Shadow Video BIOS ROM
4E	7.0	Display Copyright Notice
50	7.0	Display CPU Type And Speed
51	2.1	Initialize EISA Board
52	8.1	Keyboard Test
54	8.1	Set Key Click
58	3.1	Unexpected Interrupts Test
59	9.0	Initialize POST Display Service
5A	5.7, 7.0	Display "Press F2 To Enter SETUP"
5B	5.6	Disable CPU Cache
5C	5.1	512k to 640k RAM Test
60	5.1	Expanded Memory Test
62	5.1	Extended Memory Address Lines Test
64	2.7	Jump to User Patch 1
66	2.7	Configure Advanced Cache Registers
67	3.1	Initialize Multi-Processor APIC
68	5.6	External/CPU Cache Enable
69	2.4	System Management Mode
6A	5.6, 7.0	Display External L2 Cache Size
6B	2.7	Load Custom Defaults (optional)
6C	7.0	Display Shadow Message
6E	5.2	Display Possible Hi Addr for UMB Recovery
70	7.0	Display Error Messages
72	2.7	Check for Configuration Errors
76	8.1	Check for Keyboard Errors

Phoenix Version 4 Release 6.0 Continued		
7C	3.1, 5.4	Set Up Hardware Interrupt Vectors
7E	2.3	Initialize NPU (if present)
80	6.1	Disable Onboard Super I/O Ports & IRQs
81	6.0	Late POST Device Initialization
82	6.2	Detect/Install External RS232 Ports
83	6.4	Configure non-MCD IDE Controllers
84	6.3	Detect/Install External Parallel Ports
85	2.1	Initialize PnP ISA Devices
86	6.1	Re-Initialize Onboard I/O Ports
87	2.0	Motherboard-configurable Devices (optional)
88	5.5	BIOS Data Area Initialization
89	3.0	Enable Non-maskable Interrupts
8A	5.5	Extended BIOS Data Area Init.
8B	6.6	Test & Initialize PS2 Mouse
8C	6.5	Floppy Controller Initialization
8F	6.4	Determine Number of ATA Drives (optional)
90	6.4	Hard-Disk Controller Initialization
91	6.4	Local-Bus HD Controller Init.
92	2.7	Jump to User Patch 2
93	2.2, 2.7	Build MPTABLE for multi-processor Boards
95	6.6	Install CD ROM for Boot
96	2.2, 2.7	Clear 4 GB ES Segment Register
97	2.2, 2.7	Fix-up Multi-processor Table
98	5.4	Search for Option ROMs
99	6.6	Check for SMART Drive (optional)
9A	5.5	Shadow Option ROMs
9C	2.4	Set Up Power Management
9D	2.7	Initialize Security Engine (optional)
9E	3.1, 5.4	Hardware Interrupts Enable
9F	6.4	Determine Number of ATA & SCSI Drives

Phoenix Version 4 Release 6.0 Continued		
A0	2.5	Set Time Of Day
A2	8.3	Key Lock Test
A4	8.1	Initialize Typematic Rate
A8	7.0	Erase F2 Prompt
AA	8.1	Scan For F2 Key Stroke
AC	2.6, 7.0	Enter SETUP
AE	2.6	Clear POST Flag
B0	2.6	Check for Errors
B2	4.1	Prepare to Boot Operating System
B4	2.6	One Short Beep Before Boot
B5	4.1	Terminate Quiet Boot (optional)
B6	4.3	Password Check
B9	4.1	Prepare Boot
BA	6.6	Initialize DMI Parameters
BC	2.6	Clear Parity Checkers
BD	4.1	Display Multi-Boot Menu
BE	7.0	Clear Screen (optional)
BF	2.7	Virus/Backup Reminder Check
C0	4.1	Boot with INT 19
C1	9.0	Initialize POST Error Manager
C2	9.0	Initialize Error Logging
C3	9.0	Initialize Error Display Function
C4	9.0	Initialize System Error Handler
C5	2.7	PnPnd Dual CMOS (optional)
C6	6.6	Initialize Notebook Docking (optional)
C7	6.6	Initialize Notebook Docking Late
C8	2.4	Force Check (optional)
C9	2.7	Extended Checksum (optional)
CA		Redirect Int 15h to enable remote keyboard
CB		Redirect Int 13 to Memory Technologies Devices such as ROM, RAM, PCMCIA and serial disk.

Phoenix Version 4 Release 6.0 Continued		
CC		Redirect Int 10h to enable remote serial video
CD		Re-map I/O and memory for PCMCIA
CE		Initialize digitizer and display message
D2		Unknown Interrupt

For Boot Block in Flash ROM

Phoenix Version 4.0, Release 6

Post Code	Diag. Sect.	Description
E0	2.4	Chipset Initialization
E1	2.1	Initialize the Bridge
E2	2.4	CPU Initialization
E3	3.2	Initialize System Timer
E4	6.0	Initialize System I/O
E5	2.7	Check Force Recovery Boot
E6	4.0	Checksum BIOS ROM
E7	4.0	Go to BIOS
E8	2.7	Set Huge Segment
E9	2.2	Initialize Multi-Processor
EA	2.7	Initialize OEM Special Code
EB	3.1, 5.7	Initialize PIC and DMA
EC	5.1	Initialize Memory Type
ED	5.1	Initialize Memory Size
EE	5.5	Shadow Boot Block
EF	5.1	System Memory Test
F0	3.0	Initialize Interrupt Vectors
F1	2.5	Initialize Run-Time Clock
F2	7.0	Initialize Video
F3	2.7	Initialize System Management Mode
F4	4.1	Output One Beep Before Boot

Phoenix for Boot Block in Flash ROM Continued		
F5	4.1	Boot to Mini-DOS
F6	2.7	Clear Huge Segment
F7	4.1	Boot to Full DOS

Phoenix Medallion BIOS

See Award BIOS, Version 6

Western Digital BIOS

Post Code	Diag. Sect.	Description
01	2.2	Begin CPU Validation
02	4.0	BIOS Checksum Error
03	2.6	Shutdown
04	3.2	Interval Timer Error
05	3.2	8254 Timer Verified
06	5.1	Memory Refresh Validation Error
07	8.1	Keyboard Controller Verified
08	5.1	Verify Base Memory
09	7.0	Video Initialized
0A	5.1	Verify Memory
0B	5.7	DMA Controller 1 Verified
0C	5.7	DMA Controller 2 Verified
0D	3.1	Verify Interrupt Controller 1
0E	3.1	Verify Interrupt Controller 2
10	5.1	Memory Parity Error
11	2.6	Verify CMOS Memory
13	3.1	Initialize Interrupt
14	8.1	Keyboard Test
15	6.3	Fault in Parallel Port Initialization
16	6.2	Fault in Serial Port Initialization

Western Digital BIOS Continued		
17	5.1	Lower 640K Mem Fault
18	5.1	Mem Fault Above 1MB
19	8.1	Keyboard Configured
1A	6.5	Floppy Drive Initialized
1B	6.4	Hard Drive Initialized
1C	5.4	Game Card Initialized, if present
1D	2.3	Math Co-Processor Setup
1E	2.5	CMOS RTC Verified
1F	2.6	Calculate CMOS Checksum
21	4.0	BIOS Initialized
22	6.3	Verify Parallel Port
23	6.2	Verify Serial Port
24	2.5	CMOS RTC Verified
25	2.6	Verify Shutdown
26	5.1	Verify Calculated Memory Above 1MB
F3	2.2	CPU Verified
F9	5.2	Virtual Error

Chapter 4
BIOS Beep Codes

Some manufacturers have their BIOS emit a series of beeps indicating what part of the Post routine failed to pass. Each manufacturer has their own approach to this. Some use long and short beeps, some use low tones and high tones, and still others rely just on the number of beeps to convey the information. Unlike the hex codes though, the beep patterns tend to be consistent for each BIOS manufacturer, and do not vary from one BIOS version to the next.

Although not as definitive as the hex codes, these beep codes are still useful when troubleshooting a non-booting system, particularly when a Post Probe card is not at hand.

AMI

Beep Code	Failure
1S	(RAM) Refresh Failure
2S	(RAM) Parity Error
3S	(RAM) Base 64KB
4S	System Timer Failure
5S	CPU
6S	A-20 Failure
7S	Virtual Mode
8S	Video Memory
9S	ROM Checksum
10S	CMOS Register
11S	Cache Test
1L-3S	Memory Test
1L-8S	Display Test

Award 4.51

Beep Code	Failure
1L	Memory
1L-2S	Video Card
1L-3S	Video RAM

AST

Beep Code	Failure
1S	CPU Registers
2S	Keyboard Controller
3S	Reset Failure
4S	Keyboard Data
5S	Keyboard Input
6S	Chipset Initialization
9S	BIOS ROM Checksum
10S	System Timer Test
11S	ASIC Register
12S	CMOS RAM
1L	1st DMA Controller
1L-1S	2nd DMA Controller
1L-2S	Video, Vertical Retrace
1L-3S	Video Memory
1L-4S	Video Adapter
1L-5S	First 64KB RAM
1L-6S	Interrupt Vectors
1L-7S	Initialize Video
1L-8S	Video Memory

COMPAQ

Beep Code	Failure
1S	Passed Post (OK)
1L-1S	BIOS ROM Checksum

COMPAQ cont'd

Beep Code	Failure
2S	General Error
1L-2S	Video Adapter

EURO/MYLEX

Beep Code	Failure
1L	Start of Test
2L	Video Adapter
1L-1S-1L	Keyboard Controller
1L-2S-1L	Keyboard
1L-3S-1L	PIC 0
1L-4S-1L	PIC 1
1L-5S-1L	DMA Page Register
1L-6S-1L	RAM Refresh
1L-7S-1L	RAM Data Test
1L-8S-1L	RAM Parity Check
1L-9S-1L	1st DMA Controller
1L-10S-1L	CMOS RAM
1L-11S-1L	2nd DMA Controller
1L-12S1L	CMOS Battery Check
1L-13-1L	CMOS Checksum
1L-14-1L	BIOS ROM Checksum

IBM

Beep Code	Failure
1S	Start of POST
2S	Initialization Error
1L-1S	System Board
1L-2S	Video Adapter
1L-3S	EGA/VGA Adapter
3L	Keyboard Controller

IBM cont'd

Beep Code	Failure
Continuous or Repeating (Short)	Power Supply

Microid Research

The beep codes for the Microid Research BIOS are necessary to distinguish between multiple meanings for the hex codes, and for this reason are included in Microid Research's BIOS Code Table in Chapter 3.

MR BIOS (L=Low Tone, H= High Tone)

Beep Code	Failure
LH-LLL	ROM BIOS Checksum
LH-HLL	DMA Page Register
LH-LHL	Keyboard Controller
LH-HHL	RAM Refresh
LH-LLH	1st DMA Controller
LH-HLH	2nd DMA Controller
LH-LLLL	First 64KB Pattern Test
LH-HLLL	First 64KB Parity Generator
LH-LHLL	First 64KB Parity Check
LH-HHLL	First 64KB Data
LH-LLHL	First 64KB Address
LH-HLHL	First 64KB Block Read
LH-LHHL	First 64KB Block Write
LH-HHHL	PIC 1
LH-LLLH	PIC 2
LH-HLLH	PIC 1 Address Failure
LH-LHLH	PIC 2 Address Failure
LH-HHLH	PIC Address Error
LH-LLHH	PIC 1 Stuck Interrupt
LH-HLHH	PIC 2 Stuck Interrupt

MR BIOS Continued

Beep Code	Failure
LH-LHHH	PIT IRQ Failure
LH-HHHH	PIT 1
LH-LLLLH	PIT 2
LH-HLLLH	PIT Output Failure
LH-LHLLH	CMOS RAM
LH-HHLLH	RTC Interrupt
LH-LLHLH	Video ROM Checksum
LH-HLHLH	Keyboard Controller
LH-LHHLH	RAM Parity Error
LH-HHHLH	I/O Channel Error
LH-LLLHH	A-20 Timeout Error
LH-HLLHH	A-20 Stuck Disabled
LH-LHLHH	A-20 Stuck Enabled

Phillips

Phillips beep codes are the binary-coded equivalent of the POST hexadecimal display, with a short beep equal to zero and a long beep equal to one.

For example, an Interrupt Controller failure causes a hex code of 35. Converting each digit to binary gives 0011 0101, and would result in the series of beeps:

long, long, short, long, short, long

Note that any zeroes on the left are truncated, so the series always starts with a long beep.

Phoenix ISA / EISA / MCA

Beep Code	Failure
1-1-2	CPU Registers
Low 1-1-2	System Board
1-1-3	CMOS

Phoenix ISA / EISA / MCA Continued

Beep Code	Failure
Low 1-1-3	Extended CMOS RAM
1-1-4	BIOS ROM Checksum
1-2-1	PIT (Interrupt timer)
1-2-2	DMA Initialization
1-2-3	DMA Page Register
1-3-1	RAM Refresh
1-3-2	First 64KB RAM
1-3-3	First 64KB, Data Line
1-3-4	First 64KB, Odd-Even Logic
1-4-1	Address Line Failure
1-4-2	First 64KB, Parity
1-4-3	Bus Timing
1-4-4	Non-maskable Interrupt
2-1-1	Bit 0, First 64KB
2-1-2	Bit 1, "
2-1-3	Bit 2, "
2-1-4	Bit 3, "
2-2-1	Bit 4, "
2-2-2	Bit 5, "
2-2-3	Bit 6, "
2-2-4	Bit 7, "
2-3-1	Bit 8, "
2-3-2	Bit 9, "
2-3-3	Bit 10, "
2-3-4	Bit 11, "
2-4-1	Bit 12, "
2-4-2	Bit 13, "
2-4-3	Bit 14, "
2-4-4	Bit 15, "
3-1-1	Slave DMA Register
3-1-2	Master DMA Register
3-1-3	Master Interrupt Mask

Phoenix ISA / EISA / MCA Continued

Beep Code	Failure
3-1-4	Slave Interrupt Mask
3-2-2	Interrupt Vector Error
3-2-3	OEM Reserved
3-2-4	Keyboard Controller
3-3-1	CMOS RAM
3-3-2	CMOS Configuration
3-3-3	OEM Reserved
3-3-4	Video Memory
3-4-1	Video Initialization
4-2-1	Timer Tick Failure
4-2-2	Shutdown Test
4-2-3	A-20 Line
4-2-4	Protected Mode Interrupt
4-3-1	RAM Address Failure
4-3-3	PIC 2 Failure
4-3-4	RTC Failure
4-4-1	Serial Port Test
4-4-2	Parallel Port Test
4-4-3	Math Coprocessor

Phoenix 4.0

Beep Code	Failure
1-1-1-3	Verify Real Mode
1-1-2-1	Get CPU Type
1-1-2-3	System Hardware Initialization
1-1-3-1	Init. Chipset with Initial POST Values
1-1-3-2	Set Initial POST Values in POST Flag
1-1-3-3	CPU Register Initialization
1-1-4-1	Init. Cache With Initial POST Values
1-1-4-3	I/O Initialization
1-2-1-1	Power Management Initialization

Phoenix 4.0 Continued

Beep Code	Failure
1-2-1-2	Initial POST Values to Alt. Registers
1-2-1-3	User Batch 0
1-2-2-1	Keyboard Controller Initialization
1-2-2-3	BIOS ROM Checksum
1-2-3-1	8254 Timer Initialization
1-2-3-3	8237 DMA Controller Initialization
1-2-4-1	Reset PIC
1-3-1-1	DRAM Refresh Test
1-3-1-3	8742 Keyboard Controller Test
1-3-2-1	Set ES Segment to Register to 4 GB
1-3-3-1	Auto size DRAM
1-3-3-3	Clear 512k Base RAM
1-3-4-1	512k Base Address Lines Test
1-3-4-3	512k Base Memory Test
1-4-1-3	CPU Bus Clock Frequency Test
1-4-2-4	Reinitialize the Chipset
1-4-3-1	Shadow System BIOS ROM
1-4-3-2	Reinitialize the Cache
1-4-3-3	Auto size Cache
1-4-4-1	Configure Advanced Chipset Registers
1-4-4-2	CMOS Values to Alternate Registers
2-1-1-1	Set Initial CPU Speed
2-1-1-3	Interrupt Vectors Initialization
2-1-2-1	BIOS Interrupts Initialization
2-1-2-3	Check ROM Copyright Notice
2-1-2-4	PCI Options ROMs Initialization
2-1-3-1	Check Video Config. Against CMOS
2-1-3-2	Initialize PCI Bus and Devices
2-1-3-3	Video Initialization
2-1-4-1	Shadow Video BIOS ROM
2-1-4-3	Display Copyright Notice
2-2-1-1	Display CPU Type And Speed

Phoenix 4.0 Continued

Beep Code	Failure
2-2-1-3	Keyboard Test
2-2-2-1	Set Key Click
2-2-2-3	Keyboard Enable
2-2-3-1	Unexpected Interrupts Test
2-2-3-3	Display "Press F2 To Enter SETUP"
2-2-4-1	512k to 640k RAM Test
2-3-1-1	Expanded Memory Test
2-3-1-3	Extended Memory Address Lines Test
2-3-2-1	User Batch 1
2-3-2-3	Configure Advanced Cache Registers
2-3-3-1	External/CPU Cache Enable
2-3-3-3	Display External Cache Size
2-3-4-1	Display Shadow Message
2-3-4-3	Display Non-Disposable Segments
2-4-1-1	Display Error Messages
2-4-1-3	Check for Configuration Errors
2-4-2-1	Real-Time Clock Test
2-4-2-3	Check for Keyboard Errors
2-4-4-1	Set Up Hardware Interrupt Vectors
2-4-4-3	NPU Test
3-1-1-1	Disable Onboard I/O Ports
3-1-1-3	Detect/Install External RS232 Ports
3-1-2-1	Detect/Install External Parallel Ports
3-1-2-3	Re-Initialize Onboard I/O Ports
3-1-3-1	BIOS Data Area Initialization
3-1-3-3	Extended BIOS Data Area Init.
3-1-4-1	Floppy Controller Initialization
3-2-1-1	Hard-Disk Controller Initialization
3-2-1-2	Local-Bus HD Controller Init.
3-2-1-3	User Batch 2
3-2-2-1	Disable A20 Address Line
3-2-2-3	Clear 4 GB ES Segment Register
3-2-3-1	Search for Option ROMs

Phoenix 4.0 Continued

Beep Code	Failure
3-2-3-3	Shadow Option ROMs
3-2-4-1	Set Up Power Management
3-2-4-3	Hardware Interrupts Enable
3-3-1-1	Set Time Of Day
3-3-1-3	Key Lock Test
3-3-3-1	Erase F2 Prompt
3-3-3-3	Scan For F2 Key Stroke
3-3-4-1	Enter SETUP
3-3-4-3	Clear POST Flag
3-4-1-1	Check for Errors
3-4-1-3	Prepare to Boot Operating System
3-4-2-1	One Beep
3-4-2-3	Password Check
3-4-3-1	Clear Global Descriptor Table
3-4-4-1	Clear Parity Checkers
3-4-4-3	Clear Screen
3-4-4-4	Virus/Backup Reminder Check
4-1-1-1	Boot with INT 19
4-2-1-1	Interrupt Handler Error
4-2-1-3	Unknown Interrupt Error
4-2-2-1	Pending Interrupt Error
4-2-2-3	Option ROM Error Initialization
4-2-3-1	Shutdown Error
4-2-3-3	Extended Block Move
4-2-4-1	Shutdown I/O Error
4-3-1-3	Chipset Initialization
4-3-1-4	Refresh Counter Initialization
4-3-2-1	Forced Flash Check
4-3-2-2	HW Status of ROM Check
4-3-2-3	BIOS ROM OK Test
4-3-2-4	RAM Test
4-3-3-1	PIC Initialization
4-3-3-3	Read In Bootstrap Code
4-3-3-4	Vector Initialization

Phoenix 4.0 Continued

Beep Code	Failure
4-3-4-1	Boot the Flash Program
4-3-4-2	Boot Device Initialization
4-3-4-3	Boot Code Read OK

QUADTEL

Beep Code	Failure
1S	Start of POST
2S	CMOS
1L-2S	Video Controller
1L-3S	Peripheral Controller

Chapter 5
POST Procedures

Each BIOS version has its own peculiarities. These include the testing sequence and also what port is used to output the codes. General guidelines for port selection are given in the Chapter One section covering the DIP switch, but more specific information is available for many BIOS versions, and is listed below.

Not all BIOS Post procedures can be monitored by the POST-Probe. Some systems send POST codes to a printer port at 278h, 378h or 3BCh. These include some IBM PS2 models and others by Olivetti, NCR and AT&T. These ports cannot be detected by the POST-Probe so no codes will be displayed for these systems. There are also systems, which do not put out codes at all. This was true of the original IBM PC, and certain BIOS versions from HP, AMI and DTK. However, the most common practice is to use port 80h, which is the default setting for the POST Probe. Unless stated otherwise below, you can probably assume that Port 80h is the right choice.

For BIOS versions that do not provide codes to the Post Probe, that card's LED indicators can still provide much useful information about what is or is not happening during the POST.

AMI

Uses Port 80h for all versions.

Award

EISA systems use 300h. Others use 80h. Some versions of Award BIOS have a Burn-In feature that will repeat the POST over and over, if a flag for this is set on the motherboard. The tip-off that this is happening is that the Reset light will blink every few seconds.

COMPAQ

Most systems use Port 84H, the rest use 380. Compaq is the only BIOS to use these ports.

HP Vectra

The various Vectra BIOS versions use a four-digit POST code. The first two digits will be displayed briefly on the POST Probe, followed by the second two digits, and then the sequence is repeated. The code will also be sent to the monitor if the video circuitry is working. If failure occurs during POST, the BIOS will emit a 4-beep error code, regardless of the error.

IBM

PS2 model 20-286 uses Port 190h. PS2 model 25 & 30 use Port 90h. MCA systems use 680h. The old IBM XT uses Port 60h, which cannot be read by the POST Probe. AT machines use the standard Port 80h. There is also an extensive set of codes, which will be sent to the monitor. These are different than the bus codes displayed by the POST Probe, and are listed in Appendix C. Display of these assumes functioning video of course, and may also require an IBM reference disk in the floppy A: drive.

Phoenix

This BIOS is used by a large number of system and motherboard manufacturers, who are allowed to modify the BIOS to their own requirements. Most of these will use Port 80h for reading the Post Codes. Now that Phoenix has acquired Award, we can probably expect future versions of both to share the same standards.

Chapter 6
IBM Error Messages

IBM PC and PS/2 systems will display 6-digit error codes on the monitor screen for problems encountered during the Post. If the errors appear at all, it indicates that the video has been initialized and that a large portion of the hardware is therefore functional. However, for later portions of the Post these codes can provide additional information that should be useful in pinpointing malfunctioning components.

IBM Code	Description
000100	System or CPU board on 90/95.
000101	System Board or PIC failed.
000102	ROM BIOS, PIT, 90/95 CPU board
000103	ROM BIOS, 2KB CMOS or PIT, CPU board on 90/95. Verify jumper is in position 2-3
000104	8259 PIC, Protected Mode failed. Check 8259, 8042.
000105	8253/4 failed or Reset command from 8042 not accepted.
000106	Converting Logic test failure.
000107	PIC/PIT failure or hot NMI on 90/95. Check memory, 8254, 8259.
000108	Bus Test failure. Check adapter cards.
000109	DMA error, Low Meg chipset failure, arbitration failure.
000110	Planar Parity error. Memory, system board.
000111	I/O Parity Error. Memory adapter or RAM chip.
000112	MCA Watchdog timeout. Adapter, system board.
000113	DMA arbitration timeout. Check any adapter, 60 or 120 MB drive, system board.
000114	External ROM error.

000115	80386 Protected Mode failure. Check 8042, PIT, PIC, CPU.
000116	80386 16/32 Bit Test failed. PIC, bus controller, 8042.
000118	System board memory.
000121	Unexpected Interrupt. Check adapter boards.
000131	Cassette Wrap failure (PC), DMA compatibility. Check drive plugs, connectors.
000132-4	DMA chips.
000152	RTC/CMOS chip, battery.
000160	Adapter ID not recognized.
000161	Battery dead or not connected, or CMOS Byte 0D incorrect.
000162	An adapter or attached hardware is failing.
000163	System CMOS options not set.
000164	Memory Size Error. CMOS, bad RAM chip or address line.
000165	System options not set, or a CMOS setting does not match BIOS equipment list.
000166	Adapter busy, not returning a Ready signal.
000167	RTC, PIT or Clock Generator.
000169	Set Configuration/Features.
000171	I/O adapter, battery, system board (90/95).
000173	Any device (90/95).
000174	Set Configuration/Features (90/95).
000191	82385 cache controller.
000194	System board, RAM riser (90/95).
000199	CMOS configuration invalid.
0001XX	Unknown, system board.
000201	System board memory.
000202	RAM address error.
000203	RAM address or refresh error.

000204	Relocated memory (run diags again).
000205	CMOS error.
000207	ROM BIOS failure.
000210	CPU board (90/95) or memory riser.
000211	Base 64K on I/O channel failed.
000215	Base memory on Card 2 failed.
000216	Base memory on Card 1 failed.
000221	ROM to RAM parity error.
000225	Wrong speed SIMM installed.
0002XX	System board, memory or memory riser.
00030X	Keyboard cable, system board.
000301	No PIT response to keyboard reset command.
000302	User-indicated error from keyboard test.
000303	Keyboard or system board error.
000304	System board error.
000305	Keyboard 5V error.
000306	System board, Aux input.
000307	Device (L40SX).
000308	Numeric keypad, system board (L40SX).
0004XX	System board, parallel port.
0005XX	Video display adapter (CGA), Model 30 system board.
0006XX	Diskette drive, cable or system board.
000601	Diskette drive or controller error.
000602	Diskette boot record error.
000604	Wrong diskette drive type installed.
000606	Diskette verify failed.
000607	Write-protected diskette.
000610	Diskette initialization failed.
000621	Bad seek, bad CRO.

000623	Sector not found.
000624	Bad address mark.
000630	Index stuck high/low in “A”.
000632	Track 0 stuck off/on in “A”.
000640	Index stuck high/low in “B”.
000642	Track 0 stuck high/low in “B”.
000650	Drive speed error.
000651,2	Format, verify failure.
000653,4	Read, write.
000655	Controller failure.
000656	Drive failure.
000662	Wrong diskette drive type installed.
000663	Wrong media type in drive.
000657	Write protect stuck (protected/unprotected).
000658	Change line stuck.
000660	(changed/unchanged).
0007XX	NPU, CPU board.
0009XX	Parallel printer adapter.
0010XX	2nd parallel printer adapter.
0011XX	Primary serial port – serial device, system board.
001101	Async error or 16550 error.
001102	Card selected feedback error.
001103	Port 102H failed register check.
001106	Serial option cannot be turned off.
001107	Serial device cable.
001108,9	Async IRQ3 / IRQ4 error.
001110	16550 register failure.
001111,2	Internal / external 16550 wrap.
001113,4	16550 transmit / receive error.

001115	16550 receive data not matching transmit data.
001116	16550 interrupt error.
001117	16550 failed baud rate test.
001118	16550 interrupt wrap.
001119	16550 FIFO error.
0012XX	Dual async ad, att device, 2nd serial port.
001301	Game adapter / joystick.
0014XX	Printer error or printer port, system board.
001401	Printer test failure.
001402	Printer signaling not ready.
001403	'No paper' error, interrupt failure.
001404	System board timeout.
001405	Parallel adapter.
001406	Adapter presence test.
0015XX	SDLC adapter.
0016XX	36 / 38 workstation adapter.
0017XX	ST506 fixed disk controller.
001701	Fixed disk post error.
001702	Fixed disk adapter error.
001703	Fixed disk error.
001704	Fixed disk, cables or adapter error.
001750-2	Drive verify / read / write.
001754	Seek test error.
001755	ST506 fixed disk controller.
001756	ECC test error.
001757	Head select test error.
001780,1	Fixed disk 0 / 1 timeout.
001782	Fixed disk controller error.
001790,1	Fixed disk 0 / 1.

0018XX	Expansion chassis (PC, XT).
001803	System board (8587).
0020XX	Bisync adapter (PC), video memory (90/95).
0021XX	Alt bisync adapter.
0022XX	Cluster adapter.
0023XX	Plasma adapter error.
0024XX	EGA adapter (XT,AT), LCD display (L40SX).
002401	Planar video display, cable connectors.
002402	Video planar, 8512.
002409	Display.
002410	System board.
0026XX	XT370 emulator card, 3278/9 emulator adapter.
0027XX	XT370 emulator adapter.
0029XX	Color printer (5182).
0030XX	PC network adapter.
003001	Adapter CPU.
003002	Adapter ROM.
003003	Adapter ID, jumpers.
003004	Adapter RAM.
003005	HIC. Check cable, translator OK.
003006	+/- 12V failure.
003008	Host detected HIC failure.
003012	Card not present.
003013	Digital failure.
003016	Analog failure.
003041,2	Hot carrier.
0031XX	Alt PC network adapter.
0032XX	Display adapter PC 3270, AT3270.
0035XX	Enhanced 5250 emulation adapter.

0036XX	GPIB adapter.
0037XX	System board, fixed disk, cable.
0038XX	Data acquisition adapter.
0039XX	Professional graphics adapter.
0045XX	IEEE488 adapter.
0046XX	Multiport adapter or associated hardware.
004611	Multiport interface board.
004612,3	Multiport memory module.
004630	Multiport interface board.
004640,1	Multiport memory module.
004650	Multiport interface cable.
005001, 005017	L40SX board or LCD assembly.
005018, 19,20,23	L40SX system board or LCD assembly.
005030-3, 005037	L40SX external display or system board.
005038	Ext CRT (L40SX).
0071XX	Voice communications adapter.
007435	8514/A adapter RAM jumper or adapter.
00744X	8514/A memory module.
0074XX	8514/A adapter or PS/2 display adapter (8530).
007509	Display.
007510	XGA adapter, adapter RAM.
0076XX	Personal page printer adapter.
0078XX	High speed adapter.
0079XX	3117 adapter.
0084XX	Speech adapter.
0085XX	Expanded memory expansion adapter (XMA).
0086XX	Mouse, system board.

008601	Mouse.
008602	User indicated error (from attached device).
008603	System board.
008604	System board or mouse.
0089XX	IBM music card.
0091XX	3363 optical drive / adapter.
0096XX	SCSI adapter (w/cache), any SCSI device, system board.
0100XX	Multiprotocol adapter, system board.
010001	Multiprotocol adapter not found.
010002	Card selected feedback.
010007	Multiprotocol adapter or cable.
0101XX	300/1200 internal modem, int. fax (L40SX).
0104XX	ESDI drive, controller, cables.
010400	Unknown failure.
010450	Read/write verify failure.
010451	Replace drive.
010452	Seek test failed.
010453	Wrong device type detected.
010454	Controller failure (sector buffer test).
010455,6	Controller failure.
010458	Fixed disk (integrated controller).
010459	Drive diagnostic command failed.
010460	Unknown failure.
010461	Drive format failed.
010462	Controller seek error.
010464	Primary map not readable.
010465,6	ECC error 8,9.
010467,8	Drive, soft/hard seek error.
010469	Drive, soft error count exceeded.

010470,2	Controller wrap error.
010473	Corrupt data, low level drive.
010474,9	Unknown error.
010480	ESDI fixed disk, cable, controller. Switches 2,3,5 ON with 70/115 drive.
010481	ESDI controller.
010490	Drive 0,1 read failed.
010499	Controller.
0107XX	External 360 / 1.2MB drive or adapter.
0112XX	SCSI adapter, SCSI device.
0119XX	3119 adapter.
0121XX	3/12/2400 internal modem or serial device.
0129XX	Level 2 cache (90/95) or CPU (P75).
012917	CPU card (90/95). Verify jumper in pos 1+2 (20mhz)
0137XX	System board (90/95).
0141XX	Real-time interface coprocessor portmaster/A.
014710	Video memory, CPU or system board.
014711	Plasma display card (P75).
0149XX	Plasma display adapter.
014932	External display.
014952	Plasma display assembly.
0152XX	XGA adapter, video memory module.
0161XX	Fax concentrator adaptor.
0164XX	Internal streaming tape.
016500	6157 tape adapter.
016520	6157 tape drive.
016540	6157 streaming tape drive or adapter.
0166XX	Token ring adapter (primary) system board.
0167XX	Token ring adapter (alt).

018001, 018029	Wizard adapter or adapter memory.
018031	Wizard adapter cable.
019402-8	80286 memory adapter.
0200XX	Image adapter / memory.
0208XX	SCSI device.
0210XY	SCSI device, Y = drive Y = A. 60 mb D. 160 mb B. 80 mb E. 320 mb C. 120 mb F. 400 mb U. Undetermined drive type
0211XX	Sequential access (SCSI 2.3GB tape drive).
0212XX	SCSI printer.
0213XX	SCSI processor.
0214XX	WORM drive.
0215XX	SCSI CD-ROM drive.
0217XX	Optical memory.
0218XX	Changer (multi CD tray or juke box).
0219XX	SCSI communications device.

Chapter 7
The Legacy POST Probe

For customers still using the original (pre-PCI) Post Probe cards, this chapter explains the differences and unique features of the card. While the old cards do not monitor the PCI bus, they are still functional and powerful tools in a troubleshooting arsenal.

The Post codes displayed are exactly the same ones listed in this manual, and the voltages and other signals monitored on the ISA bus are also the same, except that the Memory Read and Memory Write are indicated by the same LED. On the other hand, the Osc and Clk signals have two LEDs each, which light alternately. The +3.3V is missing of course, since that only occurs on the PCI bus.

The card works in both ISA and EISA, and can also monitor the IBM Micro-channel machines, by using the same MCA adapter as the new card, available from Micro 2000.

The Probe

One feature unique to the old card is a tri-state logic probe, which is the source of the 'probe' in the name Post Probe. This probe is used to sample the signal outputs on the pins of any CMOS or TTL logic chips.

The probe feature was discontinued in the new version, primarily because of the trend to large scale integration, where more and more circuitry is combined into fewer and fewer chips. As this trend continues, it not only becomes less feasible to monitor signals, which are now completely inside the chips, it is also less practical to replace the chips. Many of these large integrated circuits are surface-mounted parts, which can only be removed and installed with specialized equipment.

However, if you find yourself working on a system that is old enough to have some discrete chips for the various motherboard functions, Appendix B has a list of the more common chip designations for these functions.

Using The Probe

The probe itself is an insulated lead about 2 ½ feet long, with a banana jack on one end and the probe tip on the other.

To use the probe, insert the banana jack into a matching banana plug near one edge of the Post Probe card. Insert the card into any vacant ISA slot, and turn on the system. Now the test tip can be placed on any integrated circuit pin you wish to monitor. If you are monitoring signals which transition during the Post, it might be better to place the tip on the appropriate pin before turning on the power, so that the transition can be observed.

The results can be seen on one of the three LEDs just above the banana plug, labeled HI, TRI and LOW.

HI	=	above 2.6 VDC
TRI	=	between 1.5 and 2.6 VDC
LOW	=	less than 1.5 VDC

Voltages of –5 VDC and –12 VDC are shown by lighting both the HI and LOW indicators at the same time.

The probe is designed to be used with voltages up to 12 VDC, but can be damaged by voltages higher than +12 VDC or lower than –12 VDC.

Appendix A

ISA BUS DIAGRAM

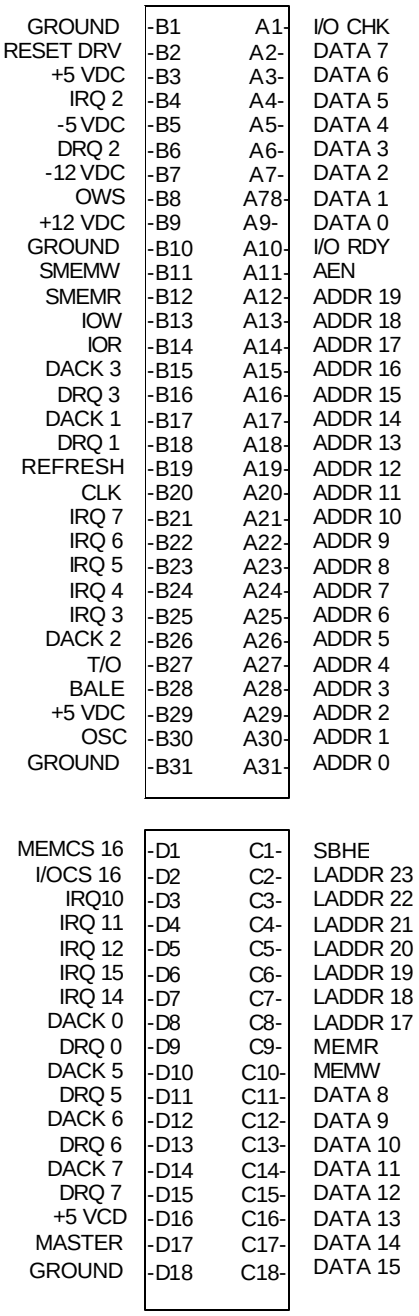
PCI BUS DIAGRAM

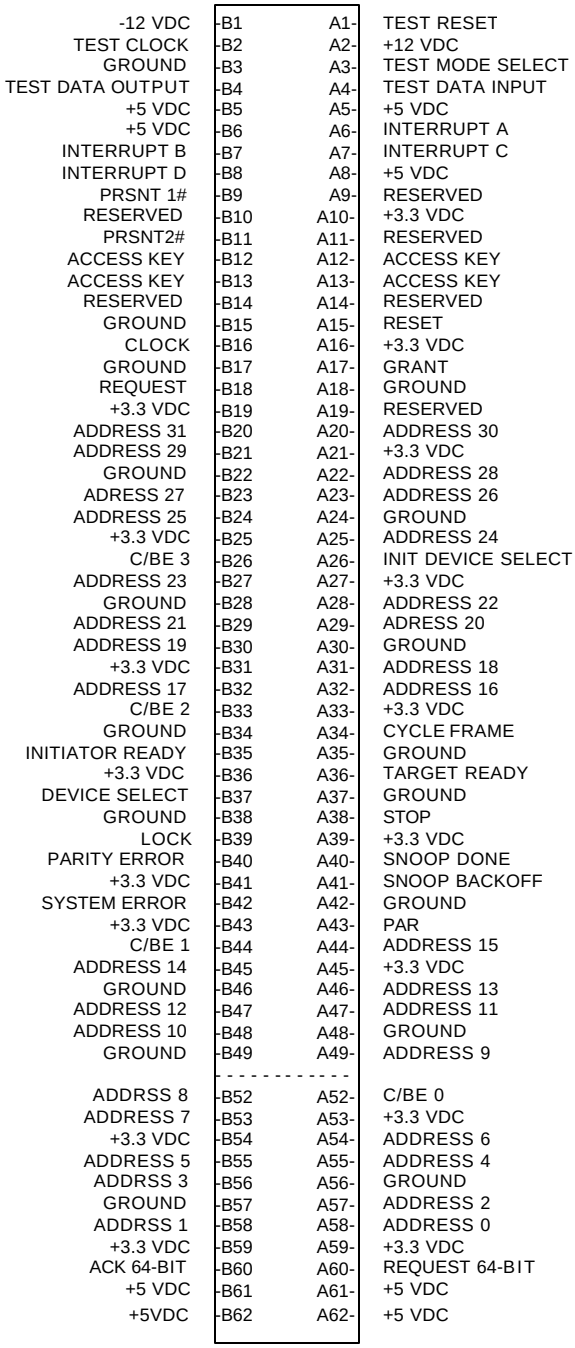
STANDARD INTERRUPTS

MEMORY ALLOCATIONS

COMMON MOTHERBOARD CHIPS

ISA BUS DIAGRAM


GROUND -B1 A1- I/O CHK
RESET DRV -B2 A2- DATA 7
+5 VDC -B3 A3- DATA 6
IRQ 2 -B4 A4- DATA 5
-5 VDC -B5 A5- DATA 4
DRQ 2 -B6 A6- DATA 3
-12 VDC -B7 A7- DATA 2
OWS -B8 A78- DATA 1
+12 VDC -B9 A9- DATA 0
GROUND -B10 A10- I/O RDY
SMEMW -B11 A11- AEN
SMEMR -B12 A12- ADDR 19
IOW -B13 A13- ADDR 18
IOR -B14 A14- ADDR 17
DACK 3 -B15 A15- ADDR 16
DRQ 3 -B16 A16- ADDR 15
DACK 1 -B17 A17- ADDR 14
DRQ 1 -B18 A18- ADDR 13
REFRESH -B19 A19- ADDR 12
CLK -B20 A20- ADDR 11
IRQ 7 -B21 A21- ADDR 10
IRQ 6 -B22 A22- ADDR 9
IRQ 5 -B23 A23- ADDR 8
IRQ 4 -B24 A24- ADDR 7
IRQ 3 -B25 A25- ADDR 6
DACK 2 -B26 A26- ADDR 5
T/O -B27 A27- ADDR 4
BALE -B28 A28- ADDR 3
+5 VDC -B29 A29- ADDR 2
OSC -B30 A30- ADDR 1
GROUND -B31 A31- ADDR 0
MEMCS 16 -D1 C1- SBHE
I/OCS 16 -D2 C2- LADDR 23
IRQ10 -D3 C3- LADDR 22
IRQ 11 -D4 C4- LADDR 21
IRQ 12 -D5 C5- LADDR 20
IRQ 15 -D6 C6- LADDR 19
IRQ 14 -D7 C7- LADDR 18
DACK 0 -D8 C8- LADDR 17
DRQ 0 -D9 C9- MEMR
DACK 5 -D10 C10- MEMW
DRQ 5 -D11 C11- DATA 8
DACK 6 -D12 C12- DATA 9
DRQ 6 -D13 C13- DATA 10
DACK 7 -D14 C14- DATA 11
DRQ 7 -D15 C15- DATA 12
+5 VCD -D16 C16- DATA 13
MASTER -D17 C17- DATA 14
GROUND -D18 C18- DATA 15



-12 VDC	B1	A1	TEST RESET
TEST CLOCK	B2	A2	+12 VDC
GROUND	B3	A3	TEST MODE SELECT
TEST DATA OUTPUT	B4	A4	TEST DATA INPUT
+5 VDC	B5	A5	+5 VDC
+5 VDC	B6	A6	INTERRUPT A
INTERRUPT B	B7	A7	INTERRUPT C
INTERRUPT D	B8	A8	+5 VDC
PRSNT 1#	B9	A9	RESERVED
RESERVED	B10	A10	+3.3 VDC
PRSNT2#	B11	A11	RESERVED
ACCESS KEY	B12	A12	ACCESS KEY
ACCESS KEY	B13	A13	ACCESS KEY
RESERVED	B14	A14	RESERVED
GROUND	B15	A15	RESET
CLOCK	B16	A16	+3.3 VDC
GROUND	B17	A17	GRANT
REQUEST	B18	A18	GROUND
+3.3 VDC	B19	A19	RESERVED
ADDRESS 31	B20	A20	ADDRESS 30
ADDRESS 29	B21	A21	+3.3 VDC
GROUND	B22	A22	ADDRESS 28
ADRESS 27	B23	A23	ADDRESS 26
ADDRESS 25	B24	A24	GROUND
+3.3 VDC	B25	A25	ADDRESS 24
C/BE 3	B26	A26	INIT DEVICE SELECT
ADDRESS 23	B27	A27	+3.3 VDC
GROUND	B28	A28	ADDRESS 22
ADDRESS 21	B29	A29	ADRESS 20
ADDRESS 19	B30	A30	GROUND
+3.3 VDC	B31	A31	ADDRESS 18
ADDRESS 17	B32	A32	ADDRESS 16
C/BE 2	B33	A33	+3.3 VDC
GROUND	B34	A34	CYCLE FRAME
INITIATOR READY	B35	A35	GROUND
+3.3 VDC	B36	A36	TARGET READY
DEVICE SELECT	B37	A37	GROUND
GROUND	B38	A38	STOP
LOCK	B39	A39	+3.3 VDC
PARITY ERROR	B40	A40	SNOOP DONE
+3.3 VDC	B41	A41	SNOOP BACKOFF
SYSTEM ERROR	B42	A42	GROUND
+3.3 VDC	B43	A43	PAR
C/BE 1	B44	A44	ADDRESS 15
ADDRESS 14	B45	A45	+3.3 VDC
GROUND	B46	A46	ADDRESS 13
ADDRESS 12	B47	A47	ADDRESS 11
ADDRESS 10	B48	A48	GROUND
GROUND	B49	A49	ADDRESS 9
	- - - - - - - - - - - -		
ADDRSS 8	B52	A52	C/BE 0
ADDRESS 7	B53	A53	+3.3 VDC
+3.3 VDC	B54	A54	ADDRESS 6
ADDRESS 5	B55	A55	ADDRESS 4
ADDRSS 3	B56	A56	GROUND
GROUND	B57	A57	ADDRESS 2
ADDRSS 1	B58	A58	ADDRESS 0
+3.3 VDC	B59	A59	+3.3 VDC
ACK 64-BIT	B60	A60	REQUEST 64-BIT
+5 VDC	B61	A61	+5 VDC
+5VDC	B62	A62	+5 VDC

PCI BUS DIAGRAM

Standard Hardware Interrupts

IRQ	FUNCTION
0	SYSTEM TIMER
1	KEYBOARD CONTROLLER
2	2ND PIC CASCADE
3	SERIAL PORT COM2
4	SERIAL PORT COM1
5	PARALLEL PORT LPT2
6	FLOPPY CONTROLLER
7	PARALLEL PORT LPT1
8	REAL TIME CLOCK
9	Available (appears as IRQ 2)
10	Available
11	SCSI*
12	ONBOARD MOUSE PORT*
13	MATHCOPROCESSOR
14	PRIMARY IDE
15	SECONDARY IDE*

* Available if not used for standard function

Memory Allocations

BASE MEMORY	
00000 – 09FFFF	DOS (or available)
UPPER MEMORY AREA	
0A0000 – 0AFFFF	VIDEO GRAPHICS
0B0000 – 0B7FFF	VIDEO B/W TEXT
0B8000 – 0B8FFF	COLOR TEXT
0C0000 – 0C7FFF	VIDEO ROM BIOS
0C8000 – 0DFFFF	ADAPTER ROM
0E0000 – 0EFFFF	PS/2 ROM or FREE MEM
0F0000 – 0F5FFF	BIOS ROM
0F6000 – 0FDFFF	BIOS ROM (or IBM Tape ROM)
0FE000 – 0FFFFF	BIOS ROM
EXTENDED MEMORY	
100000 – 10FFFF	HMA (if HIMEM.SYS loaded)
110000 and up	AVAILABLE

Common Chips

CPU	INTEL	8088 286 386 486 Pentium I-IV Pentium Pro, MMX
	AMD	K5 K6 Athlon
	CYRIX	6x86
NPU		8087 80287 80387 80487
DMA CONTROLLER		8237
PIC		8259
PIT		8254
KEYBOARD CONTROLLER		8042 8742
BUS CONTROLLER		82288
I/O CONTROLLER		82C206

Appendix B

Warranty Information

Limited Hardware Warranty

The manufacturer warrants to the original purchaser of this product that the hardware shall be free from defects resulting from faulty manufacture or components for a period of one (1) year from the date of sale. Defects covered by this Limited Warranty shall be corrected either by repair or, at the manufacturer's election, by replacement. In the event of replacement, the replacement unit shall be warranted for the remainder of the original one (1) year period or thirty days, whichever is longer.

THERE ARE NO ORAL OR WRITTEN WARRANTIES, EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THOSE OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

This Limited Warranty is non-transferable and does not apply if the product has been damaged by accident, abuse, misuse, modification, misapplication, shipping to the manufacturer or service by someone other than the manufacturer. The manufacturer does not warrant that this product will meet the purchaser's requirements; it is the purchaser's sole responsibility to determine the suitability of this product for his purposes.

THE MANUFACTURER'S SOLE OBLIGATION AND LIABILITY UNDER THIS WARRANTY IS LIMITED TO THE REPAIR OR REPLACEMENT OF A DEFECTIVE PRODUCT. THE MANUFACTURER SHALL NOT, IN ANY EVENT, BE LIABLE TO THE PURCHASER OR ANY THIRD PARTY FOR ANY INCIDENTAL OR CONSEQUENTIAL DAMAGES, INCLUDING BUT NOT LIMITED TO, DAMAGES RESULTING FROM INTERRUPTION OF SERVICE AND LOSS OF BUSINESS OR LIABILITY IN TORT RELATING TO THIS PRODUCT OR RESULTING FROM ITS USE OR POSSESSION.

Notes

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